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Development of a Sag Monitoring Instrument based on an Embedded System Platform

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DEVELOPMENT OF A SAG MONITORING INSTRUMENT BASED ON AN

EMBEDDED SYSTEM PLATFORM

By

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Small size, low weight and rugged environmental specifications characterize embedded systems. PC/104 is an embedded system architecture that implements the compact version of the PC (ISA and PCI) buses. The PC/104 architecture uses 104 pins for stacking different boards and eliminates the need for card edges and backplanes. Standardizing hardware and software around PC architecture substantially reduces the development cost, time and risks involved.

The purpose of this study is to develop an environmentally rugged and portable instrument based on the PC/104 architecture for measuring and recording voltage sags as per the International Electrotechnical Commission (IEC) standards 61000-4-30 and 61000-2-8. Two different central processing units (CPU) for the instrument are evaluated in terms of hardware setup, cost and performance. The overall performance of the instrument using either CPU indicates that the instrument can be reliably used to measure voltage sags.

DEDICATION

I would like to dedicate this research to my parents, brother, sister-in-law and niece who inspired and helped me to pursue my higher education at Mississippi State University.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to all those people who provided a constant source of help and motivation throughout my work. First of all, I would like to thank my major professor and advisor Dr. Mark Halpin. I will always revere his patience, expert guidance and ability to solve intricate problems. He made my pursuit of higher education a truly enjoyable and unforgettable experience. I would also like to thank my committee members, Dr. Nick Younan and Dr. Noel Schulz for their help and valuable time they spent in reviewing this work. Finally, I would like to express my deepest appreciation to my relatives and friends in India as well as at Mississippi State University for their blessings and encouragement.

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CHAPTER I

INTRODUCTION

An embedded system can be defined as a combination of computer hardware and software and perhaps additional mechanical and other parts to perform a dedicated function. In some cases, embedded systems can be a part of a larger system or a product [1]. In a broad sense, embedded systems can be considered as computers designed for specific applications. However, there are many basic design differences between embedded systems and conventional personal computers (PCs). Some of the distinct attributes of embedded systems are [2]:

- A dedicated processor that may be specifically designed for the application.
- Application specific software that may not even use an operating system.
- Often no standard keyboard.
- Limited or no display capability.
- Designed to react to external periodic and/or aperiodic events.
- Designed to operate in a real time environment.

Embedded systems have become ubiquitous due to the wide range of functionality they provide. A recent survey on the sale of microprocessors worldwide has indicated that while the number of personal computers shipped each year exceeds 140 million units, the number of embedded microprocessors shipped each year may exceed 5 billion units [3]. These numbers suggest the overwhelming presence of embedded systems in today's technology savvy world. While the PC market has stagnated in recent years, the embedded systems market is growing every year. From an applications perspective, embedded systems can be broadly categorized into four types [2]:

1. General computing.
    - Applications similar to desktop computing but in an embedded package.
    - Video games, automatic tellers.
2. Control systems.
    - Closed-loop feedback control of a real-time system.
    - Automobiles, chemical processes, power plants, flight control.
3. Signal processing.
    - Computations involving large data streams.
    - Radar, sonar, video compression.
4. Communication and networking.
    - Telephone system, Internet.
    - Switching and information transmission.

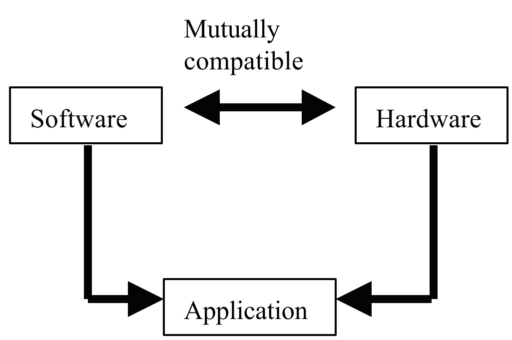
Design considerations of embedded systems

Hardware, software and application are the three design segments involved in developing an embedded system. Hardware and software segments must be compatible with each other. An application design is the integration of the hardware and software designs.

A hardware designer emphasizes processor speed, throughput, volatile and storage memories, I/O connections, power supply and other hardware used for an application.

From a software engineer's viewpoint, the operating system, compiler and programming language used for developing embedded applications are important factors. Many embedded applications are very complex in nature and need high processor speed, large volatile and storage memories, a stable operating system and high level programming language support. Finally, an application engineer must be able to combine the hardware and software features to make the embedded application work reliably and efficiently. This requires in-depth knowledge of the application and the engineering fundamentals involved. The mutual relationship between the three design phases is shown in Figure 1.1.

Figure 1.1 Design compatibility



Embedded systems are used in heterogeneous applications in vastly different environments. This fact poses some unique and challenging problems to hardware, software and application design engineers. The most important design constraints are:

- Size and weight.

- Environment.
- Power requirement.
- Cost sensitivity.
- Safety and reliability.

Embedded systems should be small in size and low in weight. In many applications, embedded systems are used in hand-held electronics, are part of a larger system or are placed in obscure locations that demand stringent size and weight requirements.

Most of the embedded systems need to operate in harsh environmental conditions like extreme temperatures, water, corrosion and vibrations. All the components in an embedded system should have proper thermal, mechanical, voltage and current ratings to withstand the application. Environmental considerations are often the most critical parameters in designing embedded systems.

Embedded system should have low power consumption. Most of the embedded applications use batteries, which have limited life. Even if an AC power supply is available, limited cooling may restrict higher power consumption.

Although embedded systems need to meet stringent requirements, cost optimization is almost always an issue. For example, components with higher thermal rating tend to be costly but a cheap piece of hardware may fail at extreme temperatures. Tradeoffs between system reliability and cost may be necessary in the hardware and application designs. There are, however, some critical applications (for example fighter planes and medical equipment) where embedded systems must operate correctly. Safety and reliability are more important issues than cost reduction in such applications.

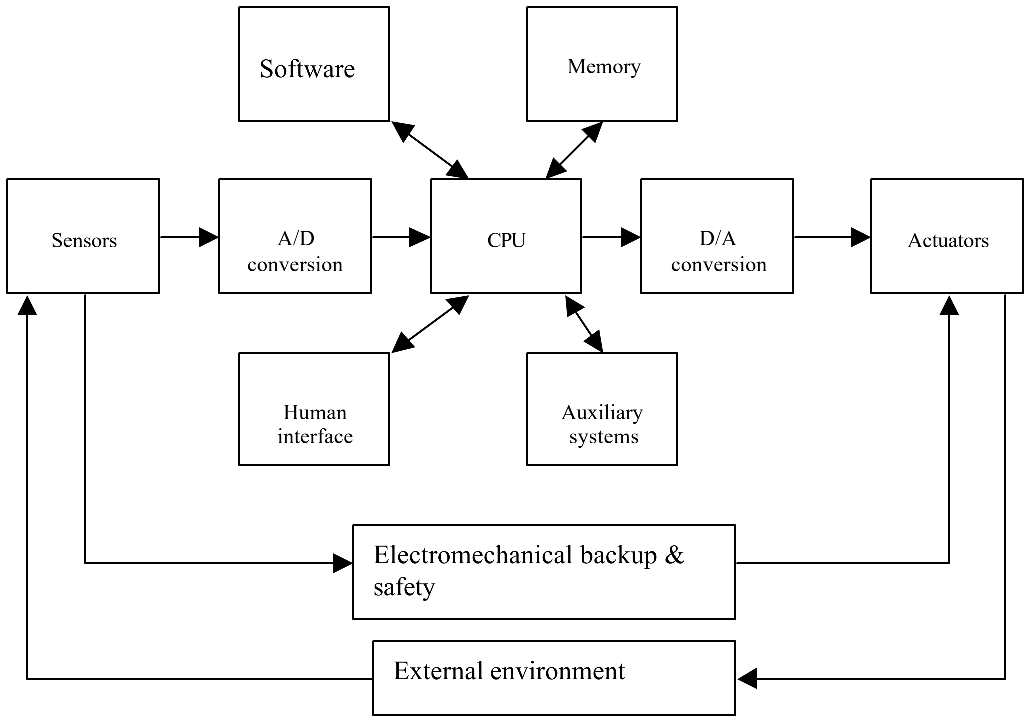
Embedded systems applications in power engineering

Embedded systems are being extensively used in different fields of power engineering. Digital relays use embedded systems for fault detection in power systems. A digital relay embedded system must be fast, intelligent, reliable and accurate to be used effectively. Unreliable operation may cause damage to equipment and personnel and false tripping. Embedded controllers are also used in speed control of motors, switch-mode power supplies and switching of capacitor banks. Any problem with the embedded system may cause mechanical and/or electrical problems in the system.

Modern revenue meters use embedded processors and data acquisition systems for measuring complex, active and reactive powers, power factor and other parameters. Such a metering system must be accurate enough to measure correct values of the quantities. Any inaccuracies will result in either customers paying higher bills or utilities losing revenues. Embedded systems are also used in monitoring and recording voltages and currents over an extended period of time. Such applications are used in collecting data for statistical studies or resolving conflicts between a utility and a customer.

Embedded systems in power applications are subjected to a wide range of operating conditions. They may be used in a control room, in a generator-turbine unit, in a sub-station or in a customer's backyard. An application designer has to choose suitable hardware and software for the intended application. Although intended for different end uses, the typical embedded system configuration for power applications remains the same. This configuration is shown in Figure 1.2

Figure 1.2 A typical embedded system organization



An embedded system can be used to monitor either single phase or three phase voltages using the setup shown in Figure 1.2. In particular, a monitor can be built to detect and record a temporary reduction in voltage(s) below a threshold at any point in an electrical system. This is discussed further in the next section.

Voltage sags – A power quality problem

Power quality can be quantified by a set of characteristics of voltages and currents at a given point on an electrical system evaluated against a set of reference parameters [4]. A power supply system can only control the quality of voltage and has no control over the currents that a load may draw. Therefore power quality of a supply system is really the quality of the supply voltage (single phase or three phase) at a given point in the system. Voltage sags, swells, harmonics, flicker and voltage unbalance (in multiphase systems) are the major power quality problems associated with supply voltages. A voltage sag (also referred to as a voltage dip) is defined as a temporary reduction of the voltage below a threshold at a point in the electrical system [4].

Voltage sags are the most common yet least avoidable power quality problem faced by utilities all over the world. In recent years, utilities have been faced with rising numbers of complaints about voltage sags. This is due to the fact that more loads are sensitive to voltage sags today than they were just a few years ago. Many applications use sensitive electronic circuitry and microprocessors. Industries are relying more and more on automated equipment to increase productivity. A voltage sag may reset controllers and the controlled process may take significant time to re-start. In some processes like semiconductor device fabrication, processes may have to be restarted all over again and a lot of raw material may be wasted. Even one voltage sag can result in significant loss in terms of productivity, time and money. Utilities and customers spend a significant amount of money and engineering effort to minimize the number of sags within their power systems.

Sag monitoring equipment can be used to measure sags and their attributes over a period of time that may vary from a few days to many months. Monitoring can be done at all the locations in a system. The data from each location can be statistically analyzed to find which locations are more vulnerable to sags and which sag locations are more detrimental to the system. A sag monitor based on an embedded system design, which can detect and record sags is the focal point of the work reported in this theses.

Scope of this research

The work which is reported in this thesis was initiated with the intent to build an environmentally rugged and portable instrument for monitoring and recording voltage sags using an embedded system architecture. The instrument was conceptualized with the following goals in mind:

1. It should be compact in size and light in weight to make it portable.
2. It should be able to withstand extreme temperatures, vibrations and physical impacts.
3. It should have almost all the capabilities that are available for a standard PC. These include:
   - A processor
   - Enough volatile memory (RAM) for application programs.
   - Sufficient storage memory to store application programs and recorded data.
   - A power supply.
   - Options for standard I/O ports, floppy drive, CD interface and network card.
   - An analog to digital data acquisition card for scanning the analog voltages.

In short, the instrument should be an embedded version of a full-blown desktop PC with data acquisition capability. It is intended to be used at any sag monitoring location, which could be an industrial plant, a commercial building, a residential location or a substation. The instrument could be placed indoors in a controlled environment or outdoors under harsh environmental conditions.

The development of this instrument is discussed in the rest of the document. Various technical terms associated with voltage sags, sag characteristics and sag-measuring methods are discussed in Chapter II. In particular, the International Electrotechnical Commission (IEC) standards for measuring voltage sags are discussed in this chapter. The method suggested in these standards was implemented on the sag-measuring instrument.

The instrument design from a hardware engineer's point of view is presented in Chapter III. PC/104, one of the most common embedded system bus architectures, different PC/104 based hardware components and their attributes are also discussed in Chapter III. Basic concepts used in data acquisition process and the data acquisition card that is used in the instrument are described in Chapter IV. Operating system, compiler and software design issues are discussed in Chapter V. The instrument design is discussed from a software engineer's point of view in this chapter. The instrument design from a power engineer's perspective is presented in Chapter VI and the testing methodology, results and their validation are discussed in Chapter VII.

CHAPTER II

VOLTAGE SAGS-A MEASUREMENT PERSPECTIVE

The two issues that must be addressed in studying voltage sags are which quantities to measure and how to measure them. IEEE does not address these measurement issues directly but the IEC standards 61000-4-30 and 61000-2-8 [4,5] give comprehensive treatment to these issues. The voltage sag measuring method recommended in these standards is implemented on the sag monitoring and recording instrument using an embedded system platform. Various technical terms and definitions used in the IEC standards for sag measurement are explained in this chapter. First, some common causes of voltage sags outlined in the IEC 61000-2-8 standard are discussed.

Causes of voltage sags

The primary causes of voltage sags are the electrical short circuits and switching of large loads that may occur throughout the electricity supply system. The short circuits are an unavoidable occurrence on power systems. A short circuit primarily involves a breakdown in the dielectric between two structures that are intended to be insulated from each other and are maintained at different potentials under normal operating conditions. The dielectric breakdown can be due to [5]:

•• Atmospheric events like lightning, wind storms, snow, and deposition of salt or atmospheric pollutants on insulators.

•• Mechanical damage due to contact by vehicles, construction equipment, excavation equipment, animals and birds, growing trees, etc.

•• Deterioration with age.

•• Switching of large loads and starting of large motors can produce large changes in currents similar to short circuit. Whatever may be the cause of a voltage sag, it can be completely described by a set of parameters and their attributes. These parameters are described in the next section.

Technical terms and definitions

Electrical quantities involved in measurement and interpretation of voltage sags are defined in the IEC 61000-4-30 standard. The technical terms and the method of measurement described in the standard make it possible to obtain reliable, repeatable and comparable results regardless of the compliant instrument being used. The technical terms used in sag measurement are:

•• Root mean square (RMS): The square root of the mean of the squares of the instantaneous values of a quantity taken over a specified time interval.

•• Voltage dip: A voltage dip or sag is a sudden reduction in voltage at a particular point on an electricity supply system below a dip threshold followed by its recovery after a brief interval. A voltage sag is a two dimensional disturbance, the level of which is determined by both voltage and time duration.

•• Dip threshold: A rms value of voltage specified for the purpose of defining the start or end of a voltage dip.

- Reference voltage: A voltage value of the supply system on which sag depths, thresholds and other values are expressed on a percentage basis.

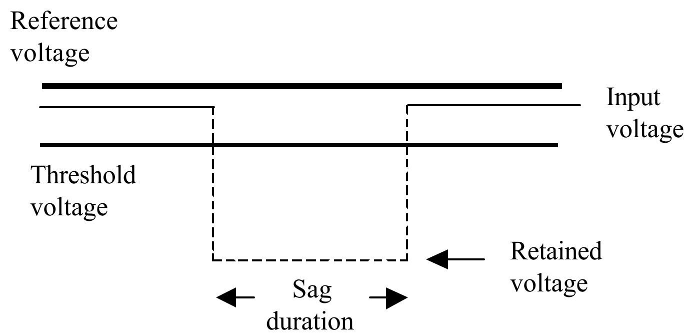
- Voltage interruption: This is a particular type of voltage dip when the voltage suddenly reduces below an interruption threshold and is restored back after a brief interval.

- Interruption threshold: This is an rms value of the voltage on an electricity system specified as a boundary such that voltage dips below this value are classified as interruptions. An interruption threshold is set to about 10% of the reference voltage and is significantly lower than the corresponding dip threshold for the system.

- RMS value of input voltage: The rms value of a voltage is measured over a cycle and refreshed each half cycle. Thus a new rms value of the input voltage can be obtained every half cycle i.e. about every 8.333 ms for a 60Hz input wave. IEC standards denote this value by $U_{rms(1/2)}$.

- Retained voltage: This is the minimum value of $U_{rms(1/2)}$ recorded during a voltage dip or interruption. Retained voltage can be expressed as a value in volts, as a percentage or per unit value of the declared input voltage. Retained voltage and the other definitions are used to explain the method of measuring voltage sags. A voltage sag is illustrated in Figure 2.1 to further clarify the definitions of reference voltage, threshold voltage, retained voltage and sag duration.

Figure 2.1 Voltage sag



Threshold voltage and retained voltage are expressed in terms of the reference voltage.

Measurement of a voltage sag

A voltage dip begins when the $U_{rms(1/2)}$ voltage falls below the dip start threshold and ends when the $U_{rms(1/2)}$ voltage is equal or above the dip end threshold. A pair of data, retained voltage and duration, characterizes a voltage dip.

The smallest value of $U_{rms(1/2)}$ measured during the dip is called the "retained voltage" and is denoted by U_{ret}. U_{ret} may be expressed either as the value to which the voltage is depressed or in terms of percentage the reference voltage.

The duration of a dip is the time difference between the beginning and the end of voltage sag. This can be expressed either in terms of the number of cycles for which a sag lasts or in milliseconds. Thus a 2-cycle 80% sag means that the sag duration was 2 cycles and U_{ret} recorded was 80% of the reference voltage. Smaller U_{ret} and longer sag duration imply a more severe sag. Sag monitors are often placed at different locations to measure these two parameters.

Voltage interruptions can also be expressed in terms of the smallest magnitude and duration. For voltage interruptions, U_{ret} magnitudes would be much smaller as compared to the sag magnitudes. For measuring voltage sags as well as interruptions, reference and threshold voltages must be set. This is considered in the next section.

Reference voltage

The reference voltage selected for sag measurements is conventionally based on the nominal or declared system voltage at the observation point. The reference voltage can be either fixed or sliding. In the case of a fixed reference, the voltage magnitude is generally the nominal or declared voltage. A fixed reference is especially useful when the matter of interest is the possible effect on utilization equipment. The voltage at the utilization equipment does not vary much from the nominal value under normal conditions. Therefore, the reference voltage for measurements on low voltage networks is usually the normal or declared voltage at the observation point.

In the case of medium and high voltage distribution networks, the nominal voltage range varies depending on the operating conditions (for example transformer tap setting) of the network at that point of time. In such networks it is preferable to measure a voltage dip relative to the preceding voltage (before the dip) to find the voltage dip. This necessitates the use of a sliding reference. In the case of a sliding reference, the voltage magnitude is averaged over a specified interval, much longer than the duration of a voltage dip, and used to represent the voltage preceding a voltage dip.

According to the IEC standard 61000-4-30, the rms value of the sliding reference voltage is calculated over a 12-cycle time window for 60Hz power systems. Each 12-

cycle interval is continuous, contiguous and non-overlapping. When a new 12-cycle interval value is available, the sliding reference is updated using equation (1):

$$U_{SR(n)} = 0.9967 \bullet U_{SR(n-1)} + 0.0033 \bullet U_{(12)r.m.s} \ldots \quad (1)$$

In equation (1), $U_{SR(n)}$ is the present value of the sliding reference voltage, $U_{SR(n-1)}$ is the previous value of the sliding reference voltage and $U_{(12)r.m.s}$ is the most recent 12-cycle rms value. The initial value of the sliding reference voltage is set to be equal to the rated or nominal voltage. The sliding reference is updated every 12-cycles when a new value of $U_{(12)r.m.s}$ is available. This corresponds to finding moving average over a 12-cycle period. The sliding reference voltage is not updated during a sag period. When a sag is over, the moving average calculation starts again.

Equation (1) is a difference equation for a first order filter with 1-minute time constant. For most of the applications, this first order filter is good enough to give a smooth sliding reference. Irrespective of the type of the reference voltage (fixed or sliding) used, threshold voltages are always setup as some percentage of the reference voltage.

Threshold voltages

As mentioned earlier, the dip threshold specifies the start and the end of a voltage dip. Typically a dip threshold is set between 85% and 95% of the reference voltage. In the case of industrial and commercial customers, the exact dip threshold depends on the contractual agreement between the electricity supplier and the customer. Allowing a margin of 10% to 15% takes into account load induced variations in nominal voltage.

This is especially relevant in the case of a fixed reference where the reference voltage does not change over the measurement period. In the case of a sliding reference, the reference voltage is available immediately before a dip and the threshold may be set to as high as 99% of the sliding reference voltage.

In many sag measuring applications, two different thresholds for detecting the start and the end of a dip are specified. The dip start threshold is set between 85% and 95% of the reference voltage. The dip end threshold is set to 1% or 2% of the reference voltage above the start threshold. Only those events in which the voltage, having fallen below the start threshold, recovers at least to the end threshold are recognized as voltage sags. The 1% or 2% extra voltage added to the end threshold makes sure that the sag event has indeed ended and the voltage has been restored within the permissible range. In some sag studies there is a particular voltage threshold which is the focus of attention, either because it is specified in the contract or because it is the value that is critical for the machine or the process involved. The start and end of the actual dip and its ultimate depth may all be irrelevant in such cases. In any case, an engineer must judiciously select start and end thresholds for a particular sag study.

The concepts of reference voltage and threshold voltages are valid in the case of multi-phase sag measurements also. For multi-phase measurements, a dip begins when the $U_{rms(1/2)}$ voltage on at least one channel falls below the dip threshold and ends when the voltages on all measured channels are equal to or above the end threshold. In some cases, it may be necessary to measure voltages between phase conductors and neutral or between phase conductors or between neutral and earth. The IEC standards do not impose any restrictions on the type of measurements. All the concepts discussed in this document are relevant to all types of measurement.

The concepts discussed in this chapter are used to implement a sag-measuring algorithm on the sag-monitoring and recording instrument. The next task is to consider the hardware requirements for building a stable platform for the sag-measuring instrument. This is done in the next chapter.

CHAPTER III

HARDWARE DESIGN ASPECTS

Choosing a bus architecture and the appropriate components that can be used on that bus is the main challenge faced by an embedded design hardware engineer. PC/104 is by far the most popular bus architecture used in developing embedded systems that implement the compact version of the PC bus. This architecture was originally proposed by Ampro Computers and has evolved around the Intel and DOS/WINDOWS architecture. At present there are over 150 vendors who manufacture PC/104 based products. Microprocessors, digital signal processors, video cards, network cards, GPS cards and almost all other application cards are available on PC/104. This bus architecture was selected for the sag-monitoring instrument. Henceforth, the discussion about embedded systems is restricted to embedded systems on PC/104 architecture. The basics of this architecture are introduced in this chapter.

Once the bus architecture has been decided, the next step is to determine the components to be used in the instrument. The basic hardware capabilities needed for the instruments are:

- Central processing unit (CPU) which is the brain of the instrument and manages system hardware and software.
- System memory. This includes random access memory (RAM) as well as storage memory for the operating system and application programs. Data acquisition card for analog to digital (A/D) conversion of input signals.
- Power supply for supplying the required power to each card in the stack.
- Other ancillary cards like video card and network cards.

Specific CPUs, system memories, power supply and other cards that were selected for the instrument are discussed later in this chapter.

PC/104 bus architecture

During the last one and a half decades, embedded applications of PCs have grown significantly and are used where devices need to be controlled by a computer. Embedded system designers soon realized the need for standardizing hardware and software around PC architecture to reduce substantially the development costs, risks and time. The hardware design and the software support were already in place for PC applications. What was lacking was a “technology transfer” medium from the PC to the embedded form factor. Industry standard bus architecture (ISA) could not be directly used for embedded applications because the standard ISA bus form factor (12.4” • 4.8”) and its associated card edges and backplanes were too bulky for embedded applications. Also, embedded systems needed lower power consumption to reduce the heat dissipated and conserve as much battery power as possible.

To address these issues, the PC/104 standard was developed. The salient features of the PC/104 standard are [6]:

- It offers full hardware and software compatibility with the ISA bus, but the form factor is 3.6” • 3.8” which much more compact than the standard ISA bus.
- The architecture uses 104 pins (and hence the name PC/104) to connect different cards together instead of card edges and plug-in slots. Boards can be stacked over each other and the bus connectivity is maintained by the 104 connector pins.
- PC/104 is an expression of a *de facto* standard (ISA), rather than the invention and design of a committee. PC/104 allows the PC’s hardware, software and system design knowledge to be fully implemented in embedded controllers.

PC/104 proved to be a groundbreaking concept in the embedded systems world. The popularity of PC/104 lies in its ability to allow a user to buy off-the-shelf hardware and customize it with software. This significantly shortens the design cycle, lowers product cost, shortens the learning curve for a user and reduces the risks involved in introducing a new product.

PC/104 cards are available in 8-bit as well as in 16-bit data bus widths. A stack of PC/104 cards can also have both (8 and 16 bit) at the same time. In recent years peripheral component interconnect (PCI) bus architecture has replaced the standard ISA bus on the PC platform. PCI bus provides a 32-bit data bus and is nearly four times faster than the ISA bus. Many PC/104 cards provide PCI bus interface along with the standard ISA interface. PC/104 standard specifies an additional 120 pins for connecting the PCI bus. Such PC/104 cards are called as “PC/104 plus” cards and are especially suitable for graphics applications. PC/104 plus cards are compatible with PC/104 cards and both types can be arranged in a stack to form an embedded system. The cards that were selected for the sag-monitoring instrument are discussed in the following specific sections.

Central Processing Unit (CPU)

Almost all the CPUs on the PC/104 architecture have a processor, RAM, ROM, onboard support for solid state memory, serial ports, parallel port, keyboard and mouse support, VGA/LCD interface, real-time clock with battery backup and status LEDs. In many PC/104 systems, RAM and storage memories may be present on separate PC/104 cards. Nonetheless, they can still be considered to be parts of a CPU. Also, the processor, CPU base board, RAM and storage memory are generally manufactured by different vendors. All the individual components can be integrated due the common platform provided by the PC/104 standard.

Processors

Processors come in different flavors depending on the manufacturer and the type of embedded applications for which they are targeted. Some common processors are AMD's 586 series, Intel's 8086 family of processors, Pentium class processors and Celeron processors. It is worth mentioning that although Intel's 8086 family of processors has become obsolete on the PC platform, it is still fairly popular on the embedded systems platform for simple and relatively slow applications. Processor frequencies vary from as low as 8MHz to as high as 700MHz. The high-end processors are capable of delivering substantially higher throughput.

Many processors have a cooling fan installed on them. This helps in dissipating the heat especially in PC/104 enclosures where air ventilation may be restricted. Because the system should be able to withstand extreme temperatures, operating temperatures of processors are a critical factor. Generally, the minimum operating temperature is not an issue. It is the maximum operating temperature that could be a cause of concern. A careful study of processor specifications is necessary before selecting a processor. Fast and large RAM is also important along with a fast processor. RAM for the sag-monitoring instrument is discussed next.

Random access memory

Dynamic random access memory (DRAM) is the preferred choice of technology for RAM as it is much cheaper and occupies much less space (on a chip) as compared to static random access memory (SRAM). The two major types of DRAM technologies are asynchronous DRAM and synchronous DRAM. In the case of asynchronous DRAM, the memory access signals are not tied to the main system clock. Each access to memory takes around 4-7 clock cycles due to the overhead involved in finding the correct memory location. SDRAM overcomes this problem by accessing the memory in what is called "burst mode access." In burst mode, the first access to memory takes the same amount of time as taken by conventional DRAM. After the initial access however four 64-bit chunks of memory are read one after the other. This significantly reduces the overhead involved in subsequent accesses to the memory. This technique requires that the memory control signals are "synchronous" with the system clock (and hence the name synchronous DRAM). Slower processors (normally speeds less than 66 MHz) use asynchronous DRAM while faster processors use SDRAM. Both types of DRAM are available on the PC/104 platform. The standard DRAM sizes (for both the types) vary from 8MB to 256MB.

While it is desirable to have faster system memory, it is more important to have large and fast caching. Having fast and large cache capability means that most of the data requests will be handled by cache instead of DRAM. This will significantly improve the CPU performance. Processors may have one or two levels of cache. Cache levels and sizes are fixed for a processor type and can not be selected as independent parameters. Most of the modern processors on a PC/104 platform have enough cache for numerical applications like sag measurement.

ADRAM as well as SDRAM were used as system memories for the sag-monitoring instrument. Operating temperature was the pivotal criterion in selecting the memory. The operating temperatures of DRAM are in the same range as those of processors. Most of the vendors sell processors and DRAM on a single board. Along with DRAM, the sag-monitoring instrument also needs mass storage memory for an operating system and application programs.

Mass storage memory

Conventional PC hard drives are sensitive to temperature, vibration and dirt and as such can not be used as mass storage devices on PC-104 systems. Also, harsh working environments of embedded systems demand a rugged storage device without any moving parts. Compact flash and DiskOnChip• (developed by M-Systems) provide ideal mass storage options.

Compact flash (also called a CF card) is the smallest removable mass data storage device available [7]. A CF card is about the size of a small matchbox and its thickness is less than one-half the thickness of a PCMCIA type-II card. CF cards use what is called "flash technology." Flash technology uses an EEPROM type of memory that does not require a battery to retain data indefinitely. CF cards are available in capacities ranging from 2 MB to 320 MB. CF cards support both 3.3V and 5V operation and their power consumption is typically 5% of the power required to operate a 2.5" disk drive. They are designed to absorb a shock from a 10-foot drop and live decades of life under typical operating conditions [7].

Another option for mass storage is DiskOnChip from M-Systems. DiskOnChip is a high performance flash memory available in a standard 32-pin DIP or 48-pin TSOP-I package (standard packages for ICs). Their capacities vary from 32MB to 288MB. DiskOnChip is managed by M-Systems patented True Flash File System (called True FFS) technology [8]. This is a driver layer that resides between the operating system's file system and the flash memory. True FFS implements an advanced algorithm that spreads write operations, including operating system files, along the entire length of

DiskOnChip area including operating system files and ensures that all the areas of the flash are used in an equal manner. This ensures that the number of erase levels (called wear) is nearly the same for all the flash areas. This process, called “wear leveling,” significantly enhances DiskOnChip lifespan.

Many companies manufacture compact flash cards. DiskOnChip is a patented product of M-systems. Both the storage media are extensively used as storage devices in embedded systems. Both the media are environmentally quite rugged and support extended operating temperature ranges. Apart from a processor, DRAM and storage memory, embedded CPUs also provide standard I/O interfaces and devices. These are discussed in the next section.

Standard I/O interfaces

Most of the CPUs can support a standard hard drive in addition to solid state memory devices (compact flash or DiskOnChip). An IDE hard drive can be used during the development phase of an embedded application because an IDE hard drive is much cheaper than any solid state device. A floppy drive interface, COM1 and COM2 serial ports, a parallel port, a USB port, VGA/SVGA interface and keyboard and mouse interfaces are also generally provided. Most of these interfaces may not be used in an actual application, but they prove to be of immense help when developing an application. There are many vendors who manufacture CPUs with different capabilities. The exact choice of a CPU depends on the targeted application. The two CPUs that were used in the sag-monitoring application are considered next.

CPUs used in the sag-monitoring instrument

Although a large number of vendors manufacture embedded CPUs, the following two CPUs were chosen for the sag-monitoring application:

- Winsystems PCM-586, which uses an AMD 5• 86 processor.
- Advanced Digital Logic MSMP3/SEV, which uses an Intel P-III processor.

Relevant features of these two CPUs are summarized in Table 3.1.

Table 3.1 Comparison of PCM-586 and MSMP3/SEV CPUs

Parameter	PCM-586	MSMP3/SEV
Processor	AMD 5• 86	Intel Pentium III
Processor speed	133 MHz	400 MHz
DRAM type	Asynchronous	Synchronous
DRAM size	32 MB	256 MB
Cache	16 KB	256 KB
Mass storage device supported	DiskOnChip	Compact flash
Mass storage capacity	288 MB	320 MB
CRT controller	Not available	Present on the board with 4 MB video RAM
PCI bus support	Does not support	Supports PCI bus.
Processor operating temperature	-40° C to +70° C	-40° C to +50° C (can be increased up to 70° C)
DRAM operating temperature	-40° C to +70° C	-25° C to +70° C
DiskOnChip and compact flash operating temperatures	-40° C to +70° C	-40° C to +70° C
Power requirement	+5V (± 5%) at 1.3 A. (• 6.5 W)	+5V (± 5%) at 1.5 A. (• 7.5W)
Processor cooling arrangement	None	Cooling fan mounted on the processor core.
Cost of the CPU base board	• $650.00	• $1530.00
Cost of mass storage devices	$1100.00	$386.00
Total development cost	• $1700.00	• $1910.00
Weight (including mass storage devices)	• 130g	• 190g

The MSMP3/SEV has more processor speed, larger DRAM, larger cache, larger storage memory, better processor cooling capability and is superior to the PCM-586 in terms of features. The only area of concern for MSMP3/SEV is the maximum operating temperature of 50°C. This can be increased up to 70°C by using a bigger heat sink, a cooling fan and a digital over-temperature detector like National Semiconductor's LM75 A/D temperature sensor chip. The LM75 is a programmable temperature sensor in which an upper threshold temperature can be set. It can be queried by the host system at any time to check the temperature. Also, it sends an interrupt to the processor when the temperature exceeds the threshold. The circuit can also be designed to switch on a fan or a warning system when the threshold is crossed [9].

As indicated in Table 3.1, the MSMP3/SEV CPU baseboard is more expensive than the WinSystems CPU but a DiskOnChip (used on the WinSystems processor) costs significantly more than a compact flash. The overall development cost of a CPU on Advanced Digital Logic platform is roughly $210 more than the development cost on WinSystems platform for the sag-monitoring instrument. This leads to a cost versus design issue. An extra $210 may be worth the price for the better features provided by the MSMP3/SEV, but some of the features like PCI bus interface were not used in the instrument. Even with low speed and limited features, the WinSystems CPU should be fast enough to calculate $U_{rms(1/2)}$ (defined in Chapter II) every half a cycle (approximately 8.333 msec) of a 60 Hz sine wave. Additional facilities like plotting sag data and accessing sag data through a remote login will definitely need a faster CPU like the

MSMP3/SEV. Considering all these issues, the sag-monitoring instrument was developed on both the CPU.

The cost estimates shown in Table 3.1 are relevant only to the configurations chosen. Any changes in the configurations (for example using a Celeron processor instead of a Pentium, using DiskOnChip on a separate PC/104 card with the MSMP3/SEV etc.) will change the cost estimates. Component specifications, their costs, features provided by the CPUs and future expansion in the instrument capabilities were the core issues in the CPU selection. Power supply, video and network cards for the instrument are discussed in the next section.

Power supply, video and network cards

A large number of power supply cards are available on PC/104 architecture. Most of these are DC/DC power supplies with a wattage rating varying from a few watts to tens of watts. DC/DC power supplies are popular because most of the PC/104 applications are placed where it is not feasible to have standard AC main power supply. This necessitates using a set of batteries in most of the embedded applications. Vendors use improved heat sink technologies and PCB designs to dissipate heat efficiently. Some power supply designs even eliminate the need of a heat sink making them lighter in weight. All power supply cards have pins for the ±5V and ±12V commonly required for various PC/104 I/O devices.

Microcomputer Systems Inc. is the only vendor to date who designs PC/104 power supplies that work with 60Hz, 120V AC input. Their power supply module MSI-NC0070 proved to be very convenient in the development stage of the instrument as it eliminated the need to use batteries or a non-PC/104 standard power supply. Since 60 Hz, 120 V AC power source may be available at most of the sag-monitoring sites, this power supply card can be used for any long term sag-monitoring application. The specifications of the MSI-NC0070 are given in Table 3.2. The minimum and maximum temperature limits of the power supply card are a cause for concern but no other AC/DC card on the PC/104 platform is available in the market at this time.

Table 3.2. MSI-NC0070 power supply card features

Parameter	**Value**
Input voltage range	90 to 264 VAC
Output voltage range	+5V @ 2.0A -5V @ 0.2A +12V @ 1.0A -12V @ 0.3A
Input frequency	47 to 63 Hz.
Operating temperature	0° C to 55° C
Cost	$225
Weight	• 90g

Practical applications of the sag-monitoring instrument do not need a video display. The instrument writes a sag information in an output file. Nonetheless, it is very convenient to have a video display during the development phase of the instrument. The MSMP3/SEV CPU has an on-board video controller and does not need a separate video card for connecting a monitor. The WinSystems CPU needs a separate video card. During development of the sag-monitoring instrument, Advanced Digital Logic's MSMVGA video card was used. The important features of this video card are listed in Table 3.3.

Table 3.3 MSMVGA video card features

Parameter	**Value**
Memory	On board 1 MB DRAM
CRT monitor	VGA/SVGA
Resolution	Up to 768 • 1024 pixels, 64000 colors
Operating temperature	-25° C to +70° C
Power	+5 V @ 0.26 A (• 1.3 W)
Weight	• 100g
Cost	$214.00

The sag-monitoring instrument can be connected to a local area network or to the Internet using an ethernet card. This would allow remote access to the sag data recorded by the instrument. A user may not have to go to the actual measurement site for collecting the sag data. The only problem with this scheme is that a network connection must be available to the instrument.

As is the case with most of the PC/104 cards, there are many types of network cards available on PC/104 platform. For the sag-monitoring instrument, a PCM-NE2000 network card from WinSystems was used. Some of the features of this network card are listed in Table 3.4.

Table 3.4 PCM-NE2000 features

Parameter	**Value**
Controller board	Complies with IEEE 802.3 standards
Network protocol	TCP/IP
Network connector	Twisted pair (RJ-45)
Operating temperature	-40° C to +85° C
Power	+5V @ at 0.1 A (0.5 W)
Cost	$210.00
Weight	• 90g.

In this chapter, the important hardware components have been discussed. The CPUs, the solid state memories, the power supply and the video and network cards described can be used to build a practical sag-monitoring instrument based on the PC/104 formfactor. The only missing piece in this setup is a data acquisition card. The basic concepts used in data acquisition and the data acquisition card used in the sag-monitor are the topics of the next chapter.

CHAPTER IV

DATA ACQUISITION AND THE HARDWARE SETUP

The sag monitoring instrument needs a data acquisition card (DAC) for analog to digital (A/D) conversion of the input voltage. The data acquisition process needs hardware as well as software support. Hardware concepts involved in the data acquisition process are similar for all DACs. However, the hardware design and the driver software vary from one vendor to another. The data acquisition process was implemented in the sag monitoring instrument using the DMM-32-AT data acquisition card from Diamond Systems Corporation. The hardware specifications of this card are given in this chapter.

The hardware aspects of the data acquisition process required for the monitoring instrument and their implementation on the DMM-32-AT DAC are discussed in this chapter. In the end, two setups of the sag-monitoring instrument, one on the WinSystems CPU and the other on the MSMP3/SEV CPU are compared.

Input and output capabilities of a DAC

The input and the output capabilities that are commonly available in a DAC are analog input, analog output, digital input and digital output. The functionality of each mode is given in Table 4.1.

Table 4.1 Input and output capabilities of a DAC

DAC mode	Function
Analog input	Samples an analog waveform at a specific rate and converts each sample into an equivalent digital code.
Analog output	Generates an analog output waveform as specified by the user.
Digital input	Acts as a trigger to start analog data acquisition or sets a digital port to either a high or a low value.
Digital output	Generates a low or high voltage at a digital port.

A DAC may not support all of the operations shown in Table 4.1. For the sag monitoring instrument, analog input is used for measuring the input values of the voltages. In the analog input mode, an analog to digital converter (A/D converter) is used to sample an analog signal at a specific rate. The digital representation of the analog input signal is used for analyzing the input in a software algorithm. DAC features discussed in this chapter are applicable only to the analog input mode unless mentioned otherwise; the other features are not relevant to this work.

Analog input channels

The number of analog input channels available on a DAC determines how many analog signals can be sampled at the same time. The number of analog input channels available varies from card to card. Irrespective of the number of analog channels available, there are two common ways of connecting analog inputs. They are single-ended input connection and differential input connection.

A single-ended input is a single-wire input that is measured with respect to the data acquisition board's signal reference (usually ground). In order for the measurement to be accurate, the board's reference must be at the same potential as the source signal's reference. Usually this is accomplished by connecting the two signal grounds, but care must be taken to avoid problematic ground loops [10].

A differential input is a two-wire input that is measured by subtracting the low input from the high input. This type of connection offers two advantages:

• It allows for greater noise immunity because the noise, which is present in equal amounts and equal phase on both the inputs, is subtracted out.

• It allows for the input signal to float with respect to ground.

A differential input is preferred when the analog input signals are weak, the leads connecting the signal to the DAC are longer than 10 feet or when the signals contain a lot of noise [11]. Some DACs may not support both the input modes. Irrespective of the input mode used, each channel needs to be sampled at a specific rate. This issue is considered next.

Sampling rate

The sampling rate determines how often A/D conversions take place. This is measured in terms of number of samples acquired per second. A faster sampling rate acquires more data in a given time giving a more accurate representation of the input. However, a faster sampling rate puts more processing burden on the system hardware. The sampling rate is set by the user and should be selected depending on the nature of the input signal. In some DACs, a different sampling rate can be specified for each analog input channel.

This facilitates sampling of vastly different waveforms using different sampling rates at the same time.

Sampling rate for an application depends on the frequency content of the analog input waveform. Higher the frequency of the analog input, higher is the sampling rate required to accurately represent the waveform. Mathematically, the sampling frequency should be at least equal to the Nyquist sampling frequency, but the maximum sampling rates allowed by a DAC is a function of the hardware circuitry used.

Resolution

The number of bits that a DAC uses to represent an analog signal is called the resolution. As an example, if a DAC has 16-bit resolution, the smallest change that can be detected is $1/(2^{16})$ or 1/65536 of the full-scale input range. This smallest change results in an increase or decrease of 1 bit in the binary sample (A/D code) of an analog input.

Higher resolution breaks the allowable input signal range into a larger number of divisions allowing smaller voltage changes to be detected. Thus a DAC having 16-bit resolution would produce a more accurate digital representation of an analog signal as compared to a 12-bit card.

Range, polarity and gain

Range is the maximum input analog voltage that can be applied to a DAC. 5V and 10V are the two standard ranges provided by most of the DACs. Polarity can be either unipolar or bipolar. If the unipolar option is selected, only positive voltages (0 to +5V or 0 to +10V) can be measured. If the bipolar option is selected, positive as well as negative voltages (±5V or ±10V) can be measured. Gain is a number used to scale down the selected range. The full-scale input voltage range is thus a function of range, polarity and gain as expressed in equation (4.1).

$$\text{Full scale voltage range} = \text{(polarity) Range / Gain} \quad \text{…. (4.1)}$$

From equation (4.1), it is clear that the higher the gain, the lower the actual full-scale voltage range selected. For example, if the range is 5V, polarity is bipolar and the gain selected is 2, the actual full-scale voltage range would be ±5/2 or ±2.5V. Because the number of bits used in resolution is fixed for a DAC, selecting a lower full-scale range (or higher gain) would allow a higher precision in the result. As an illustration, full-scale input ranges and resolutions for a 16-bit DAC for various gains are shown in Table 4.2.

Table 4.2 Analog input ranges

Polarity	**Range**	**Gain**	**Full-scale range**	**Resolution**
Bipolar	5V	1	±5V	153• V
Bipolar	5V	2	±2.5V	76• V
Bipolar	5V	4	±1.25V	38• V
Bipolar	5V	8	±0.625V	19• V
Bipolar	10V	1	±10V	305• V
Bipolar	10V	2	±5V	153• V
Bipolar	10V	4	±2.5V	76• V
Bipolar	10V	8	±1.25V	38• V

As shown in Table 4.2, for a given range and polarity, choosing higher gain gives greater resolution. The values of gain (1,2,4 and 8) considered in Table 4.2 are just for illustrating the point and are by no means the only values available. Many DACs use other values of gain. Also, all the combinations of polarity, range and gain may not be valid for a particular DAC. Hardware specifications must be consulted before choosing a combination.

Analog input channels, sampling rate, resolution and full-scale ranges are features that are common to all data acquisition cards. As mentioned earlier, the sag-monitoring instrument uses the DMM-32-AT data acquisition card from Diamond Systems Corporation. The discussion in the following sections is specific to DMM-32-AT board only. The DMM-32-AT specifications are listed in Table 4.3.

Table 4.3 DMM-32-AT specifications

Parameter	**Value**
Number of analog input channels	32
Possible analog input configurations	32 single-ended,16 differential or 16 single-ended and 8 differential
Maximum conversion rate	200000 samples per second, single channel
Minimum conversion rate	About 1 sample every 11.9 hours
Resolution	16-bit (1/65536 of full scale)
Range	5V and 10V
Polarity	Unipolar and bipolar
Gain	1,2,4,8
Bipolar input ranges	±10V, ±5V, ±2.5V, ±1.25V, ±0.625V
Unipolar input ranges	0-10V,0-5V,0-2.5V,0-1.25V
Digital I/O lines available	24
Digital input voltage	Logic 0: 0.0V min,0.8V max Logic 1: 2.0V min,5.0V max
Digital output voltage	Logic 0: 0.0V min,0.33V max Logic 1: 2.0V min,5.0V max
A/D clock	Two 82C54 counters cascaded.
Clock source	10MHz on-board clock oscillator.
Power supply requirements	+5V (±10%),0.2 A (• 1W)
Operating Temperature	-40°C to +85°C
Weight	96g
Cost	$595.00

The analog input channels, range, gain and polarity can be selected through an application program. The next parameter to be considered is the analog sampling method. The DMM-32-AT provides two methods for sampling analog inputs. These sampling methods are discussed in the next section.

DMM-32-AT A/D sampling methods

Analog sampling can be done on a single channel or on multiple channels at the same time. For sampling multiple channels, the sampled channels must be consecutive. Random selection of sampling channels is not allowed by the DMM-32-AT. A sampling range in terms of high channel and low channel is specified. For sampling multiple channels, two sampling methods are provided by the board [6]. These are:

- Sequential sampling.
- Scan sampling.

In sequential sampling, each clock pulse results in a single A/D conversion on the current channel. If the channel range is set to a single channel (high channel = low channel), each conversion is performed on the same input channel. For multiple channels, after each conversion, the channel counter increments to the next channel. When a conversion is performed on the high channel, the channel counter resets to the low channel for the next conversion. The intervals between all samples are equal. Because each clock pulse results in only one channel being sampled, the effective sampling rate is the programmed sampling rate divided by the number of channels in the sampling range. For example if the sampling rate specified is 6 samples/second and 3 analog channels are sampled, then the effective sampling rate per channel would be 6/3 or 2 sample/second for each channel. Sequential sampling is preferred when low sampling rates are needed. For high speed sampling, scanning mode is preferred.

A scan is defined as a quick burst of samples over multiple consecutive channels. When an A/D clock occurs, all the channels specified are sampled in high-speed succession. There is a short delay of 5-20 microseconds between each sample in the scan but this is acceptable for most applications. Because each clock pulse causes all channels to be sampled, the effective sampling rate for each channel is the same as the programmed rate. The total sampling rate of the board would be the programmed sampling rate times the number of channels in the sampling range. As an illustration, if the programmed sampling rate is 6 samples/second and there are 3 input channels, then the effective sampling rate would be 6 • 3 or 18 samples/second.

Scan sampling is preferred for applications that need high-speed sampling. This is the sampling method used in the sag monitoring algorithm. However, high sampling rates for multiple channels add considerable overhead to the CPU and the DAC chipset. The DMM-32-AT hardware uses interrupts and a first-in-first-out (FIFO) memory buffer to sustain sampling at high speeds in the scan mode.

FIFO and interrupt operation

The DMM-32-AT uses a one kbyte FIFO memory buffer to manage A/D conversion. It is used to store A/D data between the time it is generated by the A/D converter and the time it is read by the application program. The FIFO can hold 512 samples with each being 16 bits in size.

For low-speed sampling, each time a conversion occurs, an interrupt is generated and the program reads the data from the buffer. There is always a one to one correspondence between sampling and reading. For high-speed sampling, this would prove to be inefficient due to high interrupt rates and software overhead required.

For high-speed sampling, FIFO can be used to reduce the interrupt rate and the software overhead. FIFO is enabled by selecting the number of samples to be read per interrupt. This number, called “FIFO depth” is programmable and is generally set to one half of the FIFO depth (256 samples). When the FIFO depth is reached, an interrupt is generated and multiple samples are read. This substantially reduces the interrupt rate required for high-speed sampling. To illustrate this concept, consider the following example.

Suppose that scan sampling is used with a programmed sampling rate of 50k samples/second for scanning two channels. The effective sampling rate in this case would be 50k • 2 i.e. 100k samples/second. The fastest sustainable sampling rate on the ISA bus running under DOS is around 40 K per second [9]. If FIFO is not used, then the system will not be able to sustain the sampling rate of 100k samples/second. However, if the FIFO is enabled and the FIFO depth is set to 256 samples, the interrupt rate required would be 100000/256 • 391 per second, which is easily sustainable on the ISA bus. For this reason, the FIFO feature was used in the implementation of the sag monitoring algorithm.

All the important hardware design issues have been discussed in this and the previous chapter. The final step is to integrate the hardware components to build the sag monitoring instrument. This is described in the next section.

Hardware setup

As discussed in the previous chapter, CPUs from WinSystems and Advanced Digital Logic were used to build two separate hardware platforms for the sag monitoring instrument. Tables 4.4 and 4.5 list the PC/104 cards used in these two setups.

Table 4.4 Hardware based on the WinSystems CPU

Component	Cost	Weight	Power consumption	Operating temperatures
CPU	$650.00	• 120g	• 6.5 W	-40° C to +70° C
DiskOnChip	$1100.00	• 10g	• 0.2 W	-40° C to +70° C
Video card*	$214.00	• 100g	• 1.3 W	-25° C to +70° C
DAC	$595.00	• 96g	• 1.0 W	-40° C to +70° C
Power supply	$225.00	• 90g	-	0° C to +55° C
Total	**$2784.00**	**≈416g**	**≈9.0 W**	**-**

Total number of PC/104 boards used = 4.

* Video card is used only during the development stage.

Table 4.5 Hardware based on the MSMP3/SEV CPU

Component	Cost	Weight	Power consumption	Operating temperatures
CPU	$1530.00	• 180g	• 7.5 W	-40° C to +50° C (can be increased up to 70° C)
Compact flash	$386.00	• 10g	• 0.2 W	-40° C to +70° C
DAC	$595.00	• 96g	• 1.0 W	-40° C to +70° C
Power supply	$225.00	• 90g	-	0° C to +55° C
Total	**$2736.00**	**≈376g**	**≈8.7 W**	**-**

Total number of PC/104 boards used = 3.

As indicated in Table 4.5 and Table 4.5, the two hardware are nearly the same in terms of cost, weight and power consumption. The setup using the MSMP3/SEV does not use a video card as VGA support is provided on the CPU board. Also, the network card is not considered in the basic hardware version because it was not used during the development stage. Considering the hardware selected, both platforms satisfy all the hardware design criteria outlined for the instrument in Chapter I. In particular both the setups have small size low weight and low power consumption.

Considering all the hardware, the temperature rating of the power supply card (0° C to 55° C) is the only cause of concern. In a practical implementation of the instrument, a DC/DC power supply card with an extended temperature rating could be used.

The design of the sag-monitoring instrument from a hardware designer's point of view was considered in this and the previous chapter. Two platforms based on the PC/104 form factor have been discussed. The final task is to consider the software segment of the sag-monitoring instrument. This is discussed in the next chapter.

CHAPTER V

SOFTWARE DESIGN ASPECTS

The sag monitoring instrument needs a stable software platform compatible with the hardware selected. The software platform includes an operating system, a compiler for a high level language and the driver software for the data acquisition card. The driver software must be compatible with the operating system and the high-level language chosen for the application development. Various issues regarding the choice of operating system, programming language and important features of the driver software are also discussed in this chapter.

Operating system

The DMM-32-AT driver software (called DSCUD 5.0) supports Windows 95/98,Windows NT/2000,DOS 6.22 and Linux. Windows 95/98 and Windows NT/2000 are made for full-blown desktop applications. They need storage memory on the order of 120MB, which is not a problem on a PC platform. In the case of the sag monitoring instrument, compact flash (320MB capacity) and DiskOnChip (288MB capacity) are the storage media used. Any of the Windows operating systems will occupy a significant portion (roughly 40%) of the storage memory. DOS 6.22, however, needs only about 5MB of storage space for the system files.

The only process performed by the sag monitoring instrument is data acquisition. The multi-processing and multi-tasking capabilities that are provided by the Windows platform are not required in the monitoring application. DOS 6.22, which is a single-processing and single-tasking operating system, is capable of supporting the data acquisition task.

Virtual memory uses some portion of the storage memory as “pages” of RAM (main memory). Virtual memory performs read and write operations on these pages in the storage memory. In the case of a conventional IDE hard drive, multiple read/write operations are not a problem. In the case of a compact flash and a DiskOnChip, however, write operations can be performed only a finite number of times. Repeated writing of pages on a solid state memory device will eventually lead to the failure of the device. This repeated writing operation could be avoided by using DOS 6.22 as it does not use the concept of virtual memory.

DOS 6.22 also supports Windows 3.11. This is a 16-bit operating system supported by DOS 6.22 and allows graphics-based compilers to be used for developing application programs. Windows 3.11 provides a convenient development environment on the sag monitoring instrument. There is no need to develop applications on a different system and then execute them on the instrument hardware.

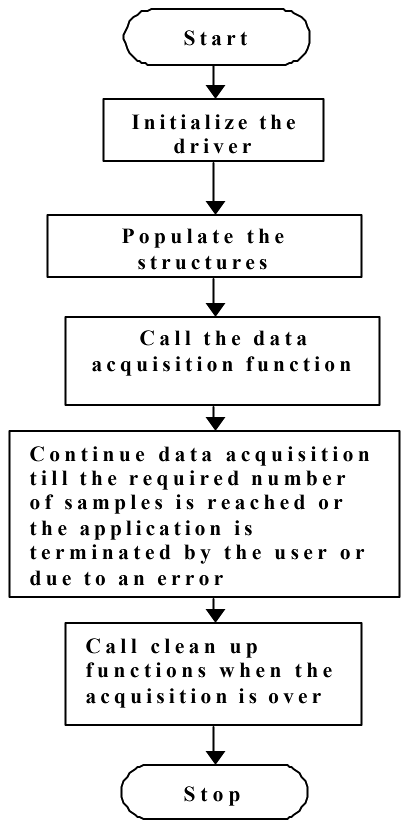
Smaller memory requirements, simple implementation and less write operations are the advantages offered by DOS 6.22. For these reasons, the DOS 6.22 operating system was chosen. The driver software implementation on DOS 6.22 is considered in the next section.

Driver software

The DMM-32-AT driver software supports C/C++ languages. The driver software is available on 16-bit as well as 32-bit platforms. Because DOS 6.22 is a 16-bit operating system, the 16-bit driver version was used. The 16-bit version of the driver software supports only Borland C compiler versions 4.5 and above. This compiler can be used on Windows 3.11. As a result the application programs were developed in C using the Borland 4.52 compiler under Windows 3.11.

The driver software uses C language structures for storing data acquisition parameters. The structures are declared in a separate driver header file. The values of data acquisition parameters are set through the application program. All the data acquisition functions are declared in the same driver header file. These functions are made available to the application through an application programming interface (API). Under DOS, the API file is statically linked with the application program. The compiler needs the driver header file, the driver API file and the application program to make the executable file. The driver software forms a middle layer between the user application and the data acquisition hardware. The user does not have to worry about the hardware implementation and can concentrate on the actual application. The generic flow of a data acquisition application program is shown in Figure 5.1

Figure 5.1 Generic flow chart of a data acquisition application program



The sag monitoring algorithm is developed using the concepts shown in Figure 5.1. The sag monitoring instrument is intended for continuous and fast acquisition of voltage data and it may run at a sag location for extended (months or years) periods. The huge amount of memory required for such applications is impossible to realize in practice, so real time data processing is required so that only relevant data is saved. The DMM-32-AT driver software allows this real time analysis by providing a double buffered data acquisition technique. This is discussed in the next section.

Double buffered data acquisition

The most common method of data acquisition is what is called "single buffering." In this type of operation, a fixed number of samples are acquired at a specific rate and transferred into computer memory for further analysis. Although single-buffered applications are simple and efficient to implement, the amount of data that can be acquired is limited to the amount of free memory available in the computer. As the monitoring instrument may need to monitor for extended periods, using single-buffered operation in continuous monitoring of data is not possible.

An alternative to single-buffered operations is double-buffered operations. In these operations, the data buffer is configured as a circular buffer of a fixed size specified by the user. When the end of the buffer is reached, data storage starts again at the beginning of the buffer; overwriting the previous data. This process can continue indefinitely until interrupted by an error or by a function call. Thus unlike single-buffered applications, double-buffered applications can acquire data points indefinitely without requiring an infinite amount of memory.

The circular data buffer is logically divided into two equal halves by the driver software. Double buffered sequential data transfer is illustrated in figures 5.2(a) through 5.2(d) [12].

Figure 5.2 (a) First half acquiring data

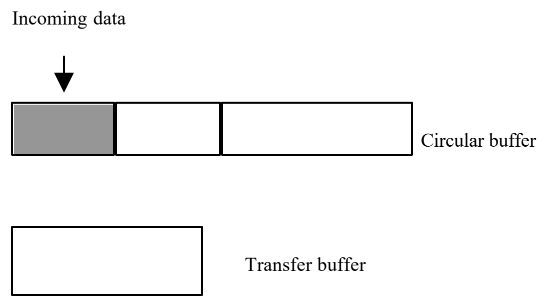


Figure 5.2 (b) Data transfer in the first half, data acquisition in the second half

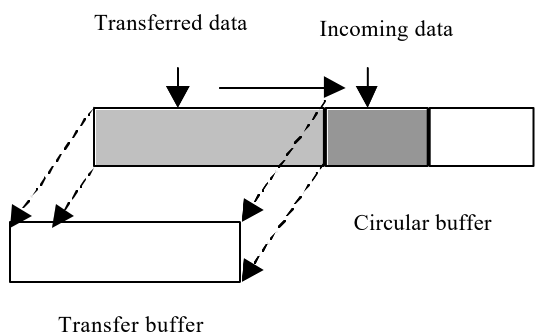


Figure 5.2 (c) Data acquisition in the first half, data transfer the second half

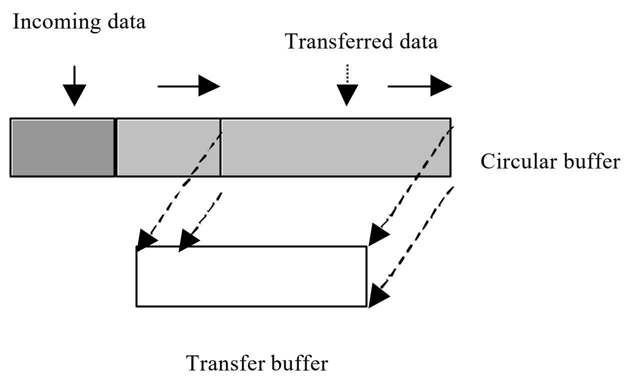
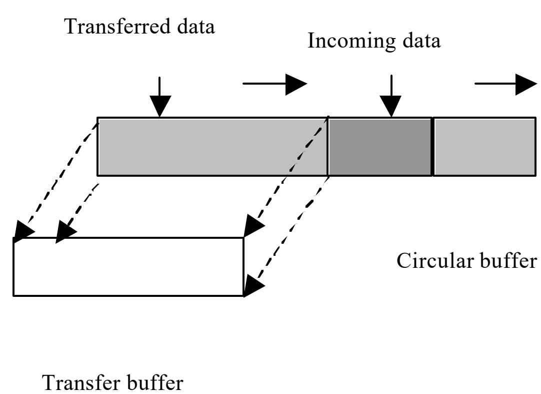


Figure 5.2 (d) Data transfer in the first half, data acquisition in the second half



The double-buffered operation begins when the DAC starts writing data into the first half of the buffer. This is shown in Figure 5.2(a). When the driver starts writing data to the second half, an interrupt is generated to signal the application program the data from the first half can be processed or stored in another buffer as needed. This is shown in Figure 5.2(b). After the second half has been filled, another interrupt is generated to indicate the application program that the second half can be utilized. The driver starts overwriting the first half of the buffer with the new data while the data in the second half is processed by the application as shown in Figure 5.2(c). This process is repeated endlessly to produce a continuous stream of data. Figure 5.2(d) is equivalent to the step shown in Figure 5.2(b).

For the double-buffered data acquisition to work correctly, the data acquisition process (in one half) must be coordinated with the data transfer process (in the other half). A mismatch between the two processes could lead to two possible errors. The first possible source of error is the DAC device overwriting the data before it is transferred to another storage location in the system memory. This results in missing data points. The second possible source of error is the DAC overwriting the data that is being simultaneously transferred. This results in a buffer having both “new” and “old” data. These two scenarios can be avoided with careful hardware and software design implementation. The processor selected should have as large a throughput (not just the speed) as possible. As far as possible, the system should have a dedicated processor for the double-buffered operations. The choice of programming language and the algorithm used for data processing also impacts the efficiency of double-buffered operations. Choice of operating system could also be one of the factors in successfully implementing a double-buffered application. The specific parameters used in the sag monitoring algorithm are discussed in Chapter VI.

In summary, the software aspects of the sag monitoring instrument have been considered in this chapter. The sag monitoring instrument uses:

- the DOS 6.22 operating system,
- the Borland 4.52 compiler,
- the C programming language,
- a driver header file defining all the data acquisition structures and functions,
- a 16-bit, statically linked API driver file and
- a double-buffered data acquisition procedures for continuous monitoring.

Hardware and software specifications of the sag monitoring instrument have been discussed in the Chapters III through Chapter V. The final step is to integrate the hardware and the software design features for the sag monitoring application. This is discussed in the next chapter.

CHAPTER VI

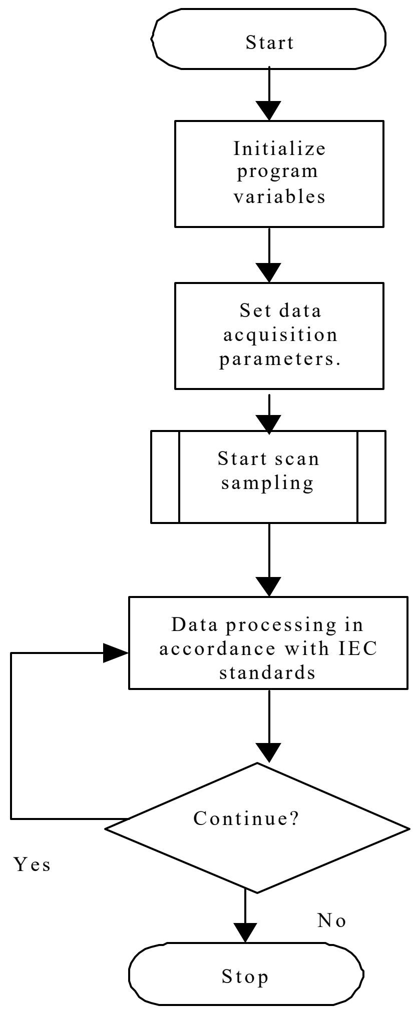
IMPLEMENTATION OF THE INSTRUMENT

All the hardware and software design issues of the sag monitoring instrument have been discussed in the previous chapters. The final step is to integrate this information and implement the sag monitoring algorithm in accordance with the IEC standards for sag measurement. The implementation of the sag monitoring algorithm is discussed in this chapter. In addition, the design aspects of the sag monitoring instrument from a power engineer's perspective are also presented in this chapter.

Sag algorithm

The sag algorithm that was used in the application program is shown in Figure 6.1. This algorithm is based on the general program structure shown in Figure 5.1.

Figure 6.1 Sag monitoring and recording algorithm



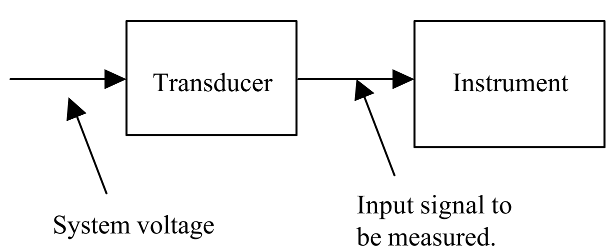
The sag monitoring algorithm was implemented for measuring sags on a 3-phase system. Each of the "process" blocks shown in Figure 6.1 uses the hardware or the software features discussed in the previous chapters. These process blocks are described in the following sections.

Setting the program variables and the data acquisition parameters

The user sets the sag threshold voltage. The application program uses a sliding reference voltage for detecting sags. The initial value of the sliding reference is also set by the user. The initial value of the sliding reference is normally set to be equal to the rms value of the nominal or rated voltage for the system.

In a practical sag monitoring application, the input voltage(s) to the instrument will be scaled down by a transducer. The transducers must be chosen such that their output signals are within the full-scale analog input range used by the application program. A block diagram of the transducer and sag monitoring instrument setup is shown in Figure 6.2.

Figure 6.2 Transducer-instrument setup



As discussed in the previous chapter, the driver software provides C structures for setting acquisition parameters. The individual structure member values are set through the application program. The data acquisition parameters that are required in the application program are summarized in Table 6.1. It should be noted that other values could be used if necessary. For example, a given hardware platform might already use IRQ 7.In this case another interrupt should be used.

Table 6.1 Data acquisition parameters used in the application program

Parameter	Value
Base address	0x300 (Hex)
Interrupt level used	7
Sampling method	Scan sampling
On board clock frequency	10 MHz
Analog input voltage range	5 V
Analog input polarity	Bipolar
Gain	1
Buffer size	96
Conversion rate	1920 Hz
Cycle mode	True
Analog input channel range (Single-ended)	0-2
FIFO	Enabled
FIFO depth	48 (Half the buffer size)

The DMM-32-AT base address and interrupt number are set by selecting the on-board jumpers. The base address and the interrupt level must also be passed to the C structure in the application program. Using the wrong base address or interrupt level in the program can cause improper operation or application failure. Interrupt conflicts between resources may also cause improper double-buffer operation. For example, interrupt level 7 is often used for a parallel port on ISA bus platforms. If a parallel port is used in the instrument, then using interrupt level 7 for data acquisition can cause erroneous scanning.

The double-buffered data acquisition is enabled by setting the cycle mode to be true. If the cycle mode is set to be false, the data acquisition will stop once the buffer is completely filled.

Channels 0,1 and 2 are used in the single-ended configuration. The range, polarity and gain parameters are set to obtain the full-scale input range from –5 V to +5 V. In a practical application, the transducer used must convert the system voltage within this range for the instrument to work properly.

The sampling rate is chosen to be 1920 Hz. Because the sampling is done in scan mode, each channel will have the same sampling rate of 1920 Hz. For a 60 Hz signal, this sampling rate corresponds to 32 (1920/60) samples per cycle (• 16.666 ms). As mentioned earlier, the sampling rate chosen must be fast enough to accurately represent the analog input waveform. For sag measuring application, the rms value of the analog input waveform is calculated every one-half cycle. 16 samples per one-half cycle (or 32 samples per cycle) are adequate to correctly represent any sub-cycle changes in the input waveform.

For 3-phase voltage sampling, the total number of samples per cycle is 96 (32 • 3). The buffer size is set to 96 samples so that one full buffer corresponds to one cycle (• • 16.666 ms) worth of data. Because the double-buffer data acquisition divides the buffer into two equal halves, each half corresponds to 48 samples, which is one-half cycle (• • 8.333 ms) worth of data for the three channels.

The effective sampling rate of the board is 5760 sample/second (1920 • 3). To keep the interrupts low, the FIFO option is enabled and the FIFO depth is set to 48 samples. The data transfer between the FIFO and the buffer will take place when the FIFO acquires 48 samples, which is one-half cycle worth of data. Because the FIFO depth is set to 48, the interrupt rate would be 120 per second (5760/48). This rate is easily sustainable.

Before calling the A/D scan sampling function, it is necessary to initialize the driver software and the hardware parameters by calling the appropriate functions. Initializing the driver software makes sure that the driver software version and the board hardware are compatible with each other. Initializing the hardware includes setting the base address, the interrupt level and the clock frequency. Calls to these functions must precede any other data acquisition function calls. Once the hardware and the software are initialized, analog sampling and scanning parameters are set.

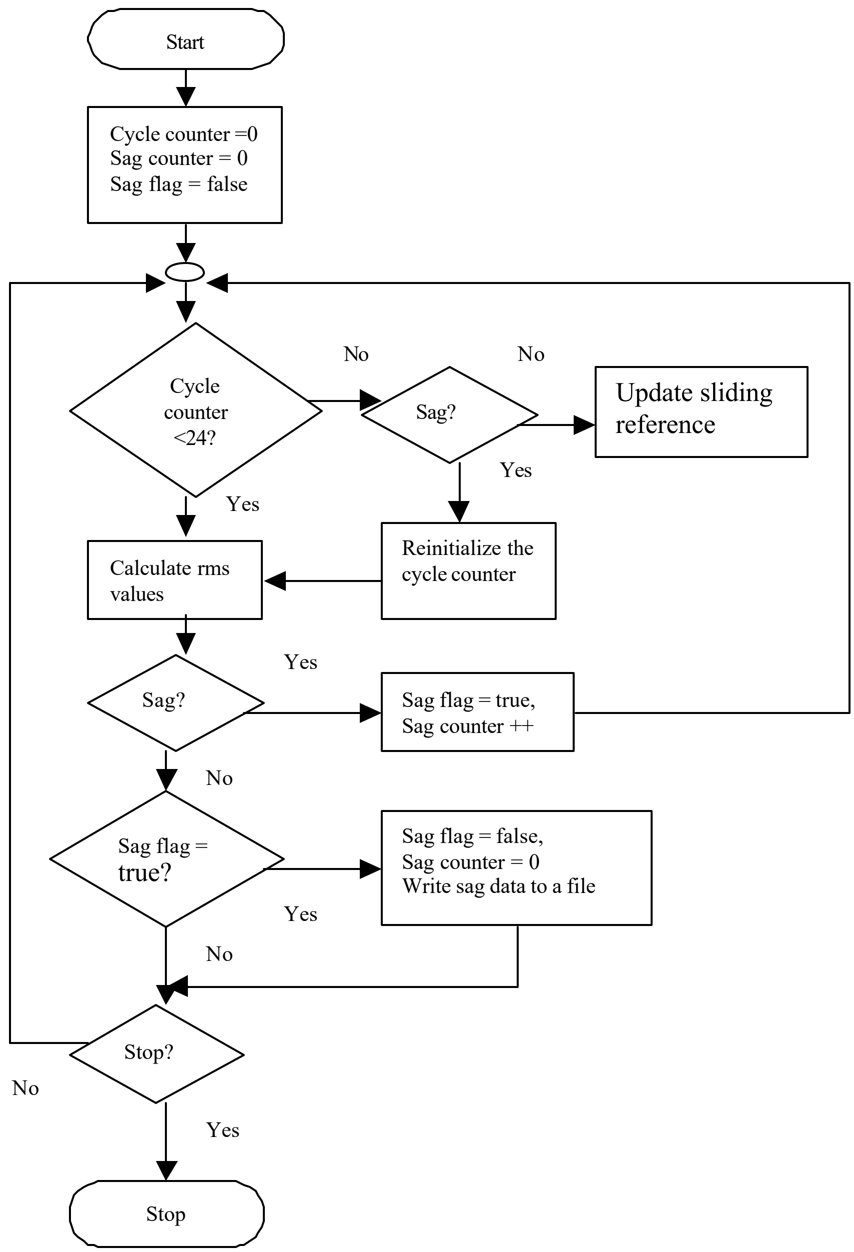
Before calling the scan sampling function, the buffer memory must be allocated. The memory allocation is done dynamically as the buffer size would vary from one application to another. In the case of the sag monitoring algorithm, the buffer size is set to 96. Each A/D sample is 2 bytes in size, so the total system memory needed for 96 samples is 192 bytes (96 • 2). If the system can not allocate the requested memory, the application is designed to stop without starting the data acquisition process. If the system does not encounter any hardware and software problems, the application program would start double-buffered data acquisition. The next process in the algorithm is to process the data in accordance with the IEC standards.

Implementation of the IEC standards in the algorithm

The initial value of the sliding reference and the voltage thresholds are set by the user. Once the double buffered data acquisition starts, the application program processes one half cycle of data for each phase at a time. The program arrays store 24 half cycles (12 cycles) worth of data for each phase. After 24 half cycles worth of data are acquired, the sliding reference value is updated using Equation (2.1) in Chapter II. The threshold value of the voltages is also updated accordingly. The application program also calculates the rms value of each input voltage every half cycle. Each rms value is compared with the voltage threshold to check if there is any sag in the voltages. If no sags occur, this process would continue indefinitely.

For a 3-phase system, a sag begins when the voltage of at least one phase falls below the start threshold and ends when the voltages of all the three phases are above the end threshold. If the application program detects a sag in any one of the input voltages, a counter is initialized and counts the number of half cycles for which the sag lasts. The minimum rms voltage recorded during the sag period on each phase is also stored. After the sag is over, the sag duration and the retained voltages for each phase are written in a text file with a date and time stamp. This sag monitoring algorithm based on the IEC standards is shown in Figure 6.3.

Figure 6.3 Sag-monitoring based on the IEC standards



In summary, the sag algorithm implementation has been discussed in this chapter. Data acquisition parameters and the program algorithm based on the IEC sag measuring standards were considered. Considering this and the previous chapters the design of the sag monitoring instrument on PC/104 platform has been discussed completely. The performance of the instrument using test waveforms is presented in the next chapter.

CHAPTER VII

INSTRUMENT PERFORMANCE

The hardware, the software and the application design phases of the sag-monitoring instrument were discussed in the Chapters II through Chapter VI. The final step is to test the instrument with voltage waveforms containing known sags. Waveforms containing known sags were generated using a programmable function generator. The instrument testing procedure and the results are presented in this chapter.

The IEC standard 61000-4-30 specifies two classes of measurement performance. These are used to benchmark the performance of the sag monitoring instrument.

Classes of performance

The IEC standard 61000-4-30 defines two classes of measurement performance. The first performance class, called Class A, is used where precise measurement is necessary. The second performance class is called Class B and is used as an indicator of performance where high accuracy is not required. Class A accuracy is used in verifying compliance with standards, resolving disputes etc. Class B indicator performance is recommended for statistical surveys, troubleshooting applications, etc. For sag measuring applications, duration and residual voltage accuracy requirements for class A and class B are given in Table 7.1.

Table 7.1 Class A and class B measurement accuracy requirements

Class A		Class B	
Duration	Residual voltage	Duration	Residual voltage
• 1 cycle • 2 cycles for interruption	• •± 0.2 %	Specified by the designer	• 2.0 %

These two classes provide benchmarks for measuring the performance of the sag monitoring instrument. It should be noted that the instrument might have different performance classes for different parameters (magnitude and retained voltage). Also, the results recorded by the instrument must be consistent i.e. measuring the same signals should produce matching results within the specified accuracy. For determining the performance class of the instrument, various test waveforms with different sag duration and retained voltage were input to the instrument. The setup for generating the test waveforms is discussed next.

Test setup for the sag-monitoring instrument

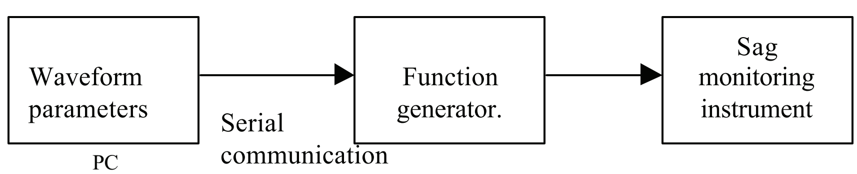
The only way to test the instrument is to test it with input sinusoidal voltages containing known voltage sags. To generate the test waveforms, Hewlett Packard's 33120A programmable function generator was used. The parameters required to program a sinusoidal voltage waveform are:

- Frequency of the input voltage.
- Peak to peak amplitude of the part of the waveform without sag.
- Number of cycles for which the sag lasts.

• Peak to peak amplitude of the part of the waveform during the sag period.

The input frequency of the test signals was set to be 60 Hz. The peak-to-peak amplitude of the part of the waveform without a sag was set at 8 V (± 4V). This is within the full-scale voltage range (±5V) of the DMM-32-AT set in the application program. The sag duration and the peak magnitude during the sag are variable parameters. Different values of the sag duration and the sag magnitudes were used to generate different waveforms. The input waveform parameters were set through a software program supported by the function generator. The function generator uses an RS-232 port for serial communication. The schematic for the test setup is shown in Figure 7.1.

Figure 7.1 Setup for testing the voltage sag instrument



Using the setup shown in Figure 7.1, various waveforms with known (programmed) sag duration and retained voltage were generated. Each duration and magnitude pair was tested repeatedly to ensure that consistent results are obtained.

Results

The monitoring instrument records the sag duration and the retained voltage. The data recorded by the instrument is compared with the known sag content. As discussed in Chapter II, the sag monitoring instrument has two different hardware setups, one using the WinSystems CPU and the other using the MSMP3/SEV CPU from Advanced Digital Logic. The sag data recorded by the instrument on the WinSystems CPU is shown in Table 7.2(a) and Table 7.2(b). The corresponding data recorded by the MSMP3/SEV CPU is summarized in Table 7.3(a) and Table 7.3(b). The known (programmed) sag duration of the test waveforms are indicated in the first column of each table. The known sag depths or the retained voltages during the sag periods are indicated in the first row of each table. Note that sag depths are expressed as a percentage of the rms value of the reference voltage. Sag duration and the percentage sag depths recorded by the instrument are indicated in the remaining rows and columns. The first row in each cell is the number of sag cycles recorded by the instrument. The second row in each cell is the retained voltage in percentage recorded by the instrument. Note that each duration and magnitude pair was tested repeatedly. The threshold voltage for all the measurements is 95% of the sliding reference.

Table 7.2(a) Sag data recorded using the WinSystems CPU

(Retained voltage varying from 90% to 50%)

Retained vol.(%)	90	85	80	70	60	50
Sag duration (cycle)						
1	0.5-2, variable	1-2, variable	1-2, variable	1-2, variable	1-2, variable	1-2, variable
2	1.5-3, 89.9-90	2-3, 84.9 – 85	2-3, 79.9-80	2-3, 69.9-70	2-3, 59.9 – 60.05	2-3, 49.9 – 50.05
3	2.5-4, 89.9 – 90	3-4, 84.9 – 85	3-4, 79.9 – 80	3-4, 69. – 70	3-4, 59.9 – 60	3-4, 49.9 – 50.05
6	5.5-7, 89.9 – 89.99	6-7, 84.9-85	6-7, 79.9 – 80	6-7, 69.9 – 70.05	6-7, 9.9 – 59.99	6-7, 49.95 – 50.0
10	9.5, 89.95 – 89.99	10-11, 84.9-85.05	10-11, 79.9 – 80	10-11, 69.9 – 69.95	10-11, 59.9 – 59.95	10-11, 49.95 – 50.05
14	13.5-15, 89.95-90.03	14-15, 84.99 – 85	14-15, 79.95 – 80	14-15, 69.95 – 70	14-15, 9.95 – 60	14-15, 49.9 – 50.05
20	19.5-21, 89.97 – 90.1	20-21, 84.99- 85.1	20-21, 80 – 80.08	20-21, 69.98 – 70	20-21, 59.98 - 60.05	20-21, 49.99 – 50.05
25	24.5-26, 9.95 – 90	25-26, 84.95 – 85.05	25-26, 79.95 – 80.05	25-26, 69.9 – 70	25-26, 59.95 – 60	25-26, 49.95 – 50.1
30	29.5-31, 90-90.1	30-31, 84.95 – 85.05	30-31, 79.99 – 80.02	30-31, 69.95 – 70.05	30-31, 59.98 - 60.03	30-31, 49.95 – 50.05
35	34.5-36, 89.99- 90.02	35-36, 85 –85.01	35-36, 79.95-80.05	35-36, 69.9-70.05	35-36, 59.98 – 60.05	35-36, 49.95 – 50.05
60	59.5-61, 90- 90.05	60-61, 84.95 –85	60-61, 79.9 –80	60-61, 69.9 –70	60-61, 59.95- 60.05	60-61, 49.95-50.05

Table 7.2(b) Sag data recorded using the WinSystems CPU

(Retained voltage varying from 40% to 0%)

Retained vol.(%)	40	30	20	10	0
Sag duration (cycle)					
1	0.5-2, variable	1-2, variable	1-2, variable	1-2, variable	1-2, variable
2	1.5-3, 39.9- 40.05	2-3, 29.95- 30.05	2-3, 19.85- 19.95	2-3, 9.93 – 10	2-3, 0.2 – 0.25
3	2.5-4, 39.95 – 40	3-4, 29.9 – 29.95	3-4, 19.9 – 19.95	3-4, 9.9- 10	3-4, 0.15 – 0.25
6	5.5-7, 39.95 – 40.0	6-7, 29.9 – 29.95	6-7, 19.95 – 20	6-7, 9.95-10	6-7, 0.15-0.25
10	9.5-11, 39.95 – 39.99	10-11, 29.9 – 29.99	10-11, 19.9 – 20	10-11, 9.9 10	10-11, 0.15-0.25
14	13.5-15, 39.95 – 40	14-15, 29.9 – 29.95	14-15, 19. 9 – 19.95	14-15, 9.9 – 10	14-15, 0.15 – 0.2
20	19.5-21, 9.95 – 40.05	20-21, 29.95 – 30.03	20-21, 19.9 – 20	20-21, 9.9 9.95	20-21, 0.1 – 0.25
25	24.5-26, 40.01 – 40. 05	25-26, 29.95- 30	25-26, 19.9 – 19.95	25-26, 9.9 – 9.95	25-26, 0.15-0.25
30	29.5-31, 39.99 – 40	30-31, 29.95 – 30.05	30-31, 19.9 – 19.95	30-31, 9.9- 9.95	30-31, 0.1 – 0.25
35	34.5-36, 39.98 – 40.05	35-36, 29.97 – 30.01	35-36, 19.9 – 19.95	35-36, 9.95 – 10	35-36, 0.15 – 0.25
60	59.5-61, 39.95 – 40.01	60-61, 29.95 – 30.05	60-61, 19.95-20.0	60-61, 9.95 – 10	60-61, 0.15 – 0.25

Table 7.3(a) Sag data recorded using the MSMP3/SEV CPU

(Retained voltage varying from 90% to 50%)

Retained vol.(%)	90	85	80	70	60	50
Sag duration (cycle)						
1	0.5-2, variable	1-2, variable	1-2, variable	1-2, variable	1-2, variable	1-2, variable
2	1.5-3, 89.9-90	2-3, 84.9 – 85	2-3, 79.9-80	2-3, 69.9-70	2-3, 59.9 – 60.05	2-3, 49.9 – 50.05
3	2.5-4, 89.9 – 90	3-4, 84.9 – 85	3-4, 79.9 – 80	3-4, 69. – 70	3-4, 59.9 – 60	3-4, 49.9 – 50.05
6	5.5-7, 89.9 – 89.99	6-7, 84.9-85	6-7, 79.9 – 80	6-7, 69.9 – 70.05	6-7, 9.9 – 59.99	6-7, 49.95 – 50.0
10	9.5, 89.95 – 89.99	10-11, 84.9-85.05	10-11, 79.9 – 80	10-11, 69.9 – 69.95	10-11, 59.9 – 59.95	10-11, 49.95–50.05
14	13.5-15, 89.95-90.03	14-15, 84.99 – 85	14-15, 79.95 – 80	14-15, 69.95 – 70	14-15, 9.95 – 60	14-15, 49.9 – 50.05
20	19.5-21, 89.97 – 90.1	20-21, 84.99- 85.1	20-21, 80 – 80.08	20-21, 69.98 – 70	20-21, 59.98 - 60.05	20-21, 49.99–50.05
25	24.5-26, 9.95 – 90	25-26, 84.95 – 85.05	25-26, 79.95 – 80.05	25-26, 69.9 – 70	25-26, 59.95 – 60	25-26, 49.95 – 50.1
30	29.5-31, 90-90.1	30-31, 84.95 – 85.05	30-31, 79.99 – 80.02	30-31, 69.95 – 70.05	30-31, 59.98 - 60.03	30-31, 49.95 -50.05
35	34.5-36, 89.99- 90.02	35-36, 85 –85.01	35-36, 79.95-80.05	35-36, 69.9-70.05	35-36, 59.98 – 60.05	35-36, 49.95 -50.05
60	59.5-61, 90- 90.05	60-61, 84.95 –85	60-61, 79.9 –80	60-61, 69.9 –70	60-61, 59.95- 60.05	60-61, 49.95-50.05

Table 7.3(b) Sag data recorded using the MSMP3/SEV CPU

(Retained voltage varying from 90% to 50%)

Retaine d vol.(%)	40	30	20	10	0
Sag duration (cycle)					
1	0.5-2, variable	1-2, variable	1-2, variable	1-2, variable	1-2, variable
2	1.5-3, 39.9- 40.05	2-3, 29.95- 30.05	2-3, 19.85- 19.95	2-3, 9.93 – 10	2-3, 0.2 – 0.25
3	2.5-4, 39.95 – 40	3-4, 29.9 – 29.95	3-4, 19.9 – 19.95	3-4, 9.9- 10	3-4, 0.15 – 0.25
6	5.5-7, 39.95 – 40.0	6-7, 29.9 – 29.95	6-7, 19.95 –20	6-7, 9.95-10	6-7, 0.15-0.25
10	9.5-11, 39.95 – 39.99	10-11, 29.9 – 29.99	10-11, 19.9 – 20	10-11, 9.9 10	10-11, 0.15-0.25
14	13.5-15, 39.95 – 40	14-15, 29.9 – 29.95	14-15, 19. 9 – 19.95	14-15, 9.9 – 10	14-15, 0.15 – 0.2
20	19.5-21, 9.95 – 40.05	20-21, 29.95 – 30.03	20-21, 19.9 – 20	20-21, 9.9 9.95	20-21, 0.1 – 0.25
25	24.5-26, 40.01 – 40. 05	25-26, 29.95- 30	25-26, 19.9 – 19.95	25-26, 9.9 – 9.95	25-26, 0.15-0.25
30	29.5-31, 39.99 –40	30-31, 29.95 – 30.05	30-31, 19.9 – 19.95	30-31, 9.9- 9.95	30-31, 0.1 –0.25
35	34.5-36, 39.98 – 40.05	35-36, 29.97 – 30.01	35-36, 19.9 –19.95	35-36, 9.95 –10	35-36, 0.15 –0.25
60	59.5-61, 39.95 – 40.01	60-61, 29.95 – 30.05	60-61, 19.95-20.0	60-61, 9.95 – 10	60-61, 0.15 –0.25

Analysis of the results

The sag measuring capability of the instrument is demonstrated in the results shown in Table 7.2(a) through Table 7.3(b). In most of the cases, the instrument records sag duration accurately within one cycle of the programmed sag duration. The retained voltages are accurate within 0.1 % to 0.2 % of the actual values. The small variation in the retained voltages is due to the imperfections in the input wave forms generated by the function generator. In some cases, the positive and negative half cycle peaks of the test waveforms were slightly different. Even a slight change in the wave shape will alter the rms value measured by the instrument.

Applying class A and class B accuracy criteria to the results tabulated in Table 7.1(a), (b) and Table 7.2 (a), (b), it can be observed that,

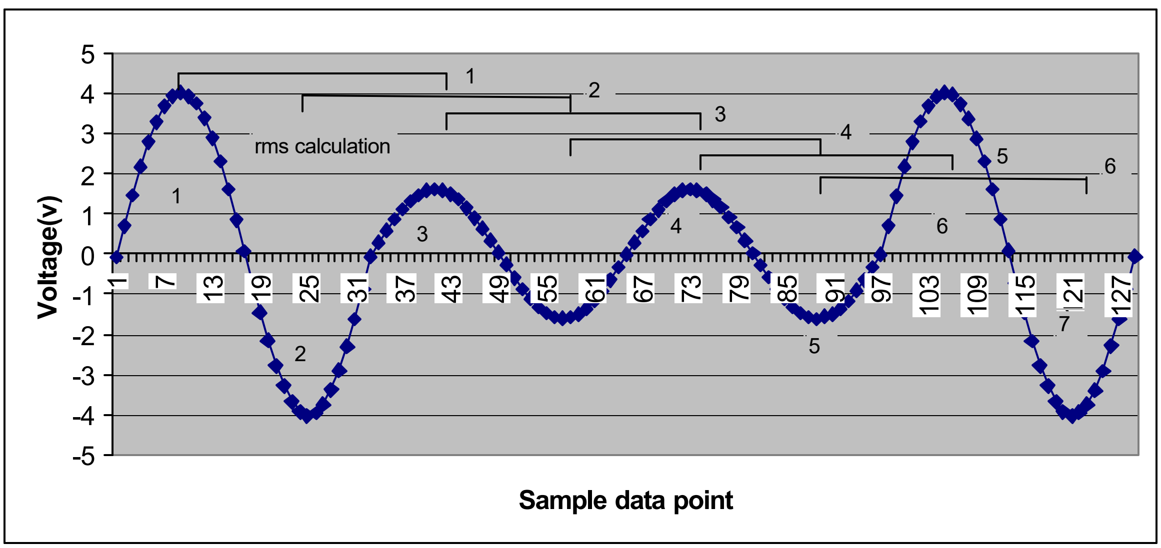
- The sag duration recorded can vary up to one cycle. The only exception is when the retained voltage is 90%. In this case sag duration recorded can vary up to one and a half cycle from the programmed sag duration. The duration accuracy of the instrument on either setup satisfies Class A performance except in the case when the retained voltage is 90%.
- Retained voltage accuracy of the instrument satisfies class A accuracy in most of the cases. But in the case of sags with one-cycle duration, the retained voltage recorded is not reliable. For any other sag duration, the retained voltages calculated are within Class A accuracy limits.

The facts that sag duration recorded by the instrument can vary and the instrument can not reliably predict the retained voltages in the case of one cycle sags need further analysis.

Variation in the sag duration

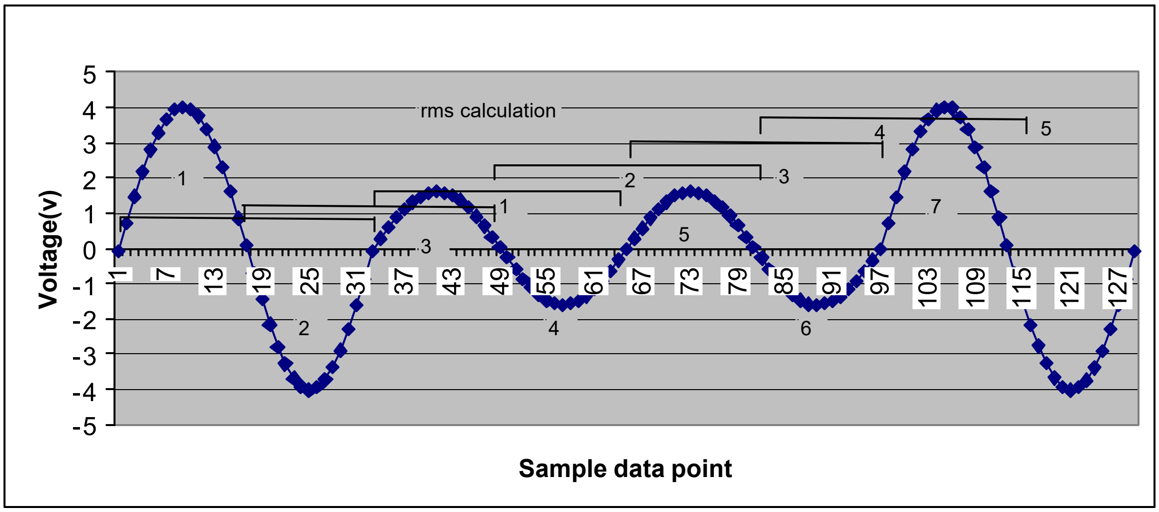
As mentioned in the last chapter, the DAC acquires 16 samples per one half cycle. Once the 16 samples are acquired, the program updates the rms value. But the data acquisition can begin at any arbitrary point on the voltage wave. There is no guarantee that the DAC would start acquiring data at zero crossing of the cycle containing sag. Due to this fact, there might be a variation of up to one cycle in the sag duration recorded by the sag. This point is clarified further with the help of Figure 7.4 and Figure 7.5.

Figure 7.2 Data acquisition not beginning at the zero crossing



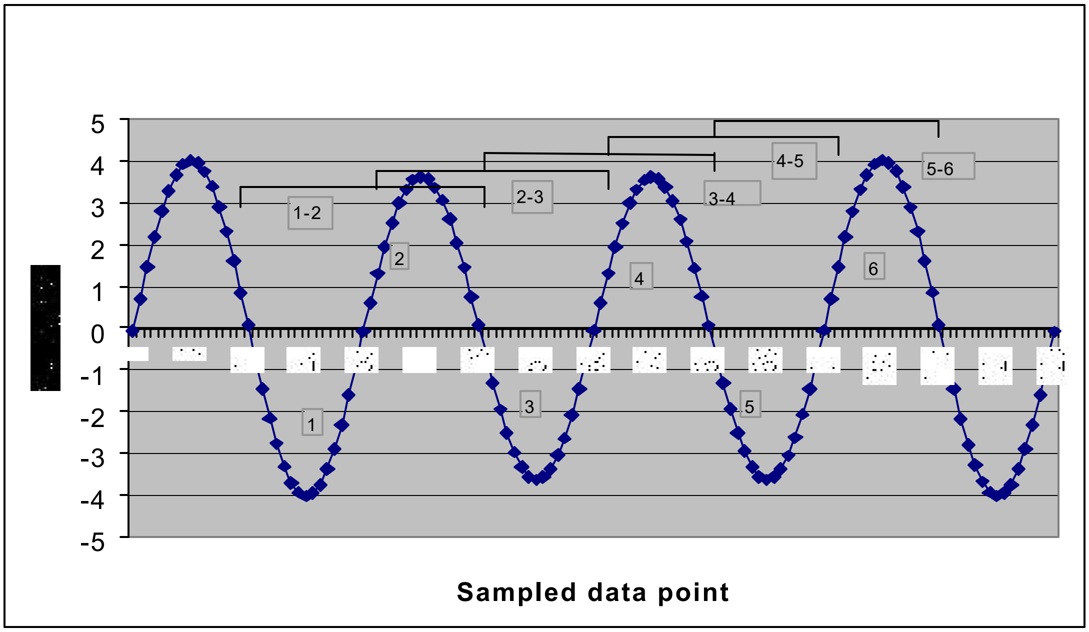
A 2-cycle, 40% retained voltage sag is shown in Figure 7.2. In the figure, the data acquisition begins at the peak of the waveform instead of at the positive going zero crossing of the waveform. The instrument will detect the sag for six half cycles or 3 cycles. But if the data acquisition begins at the zero crossing as illustrated in Figure 7.3, the sag will be measured for five half cycles or 2.5 cycles.

Figure 7.3 Data acquisition beginning at the zero crossing



In conclusion, it can be said that depending on the point on the waveform where the data acquisition begins, the sag duration recorded will vary up to one cycle. The fact that sag duration recorded by the instrument may be longer by up to a cycle is not a cause for concern. Class A sag duration accuracy is one cycle and the instrument still meets this performance accuracy. Also, the instrument will never record a sag duration that is shorter than the actual sag. Therefore, variations in the sag duration if any, will be on the conservative side. The fact that the sag duration recorded in the case of 90% retained voltage is investigated next.

Figure 7.4 2 cycle sag with 90% retained voltage



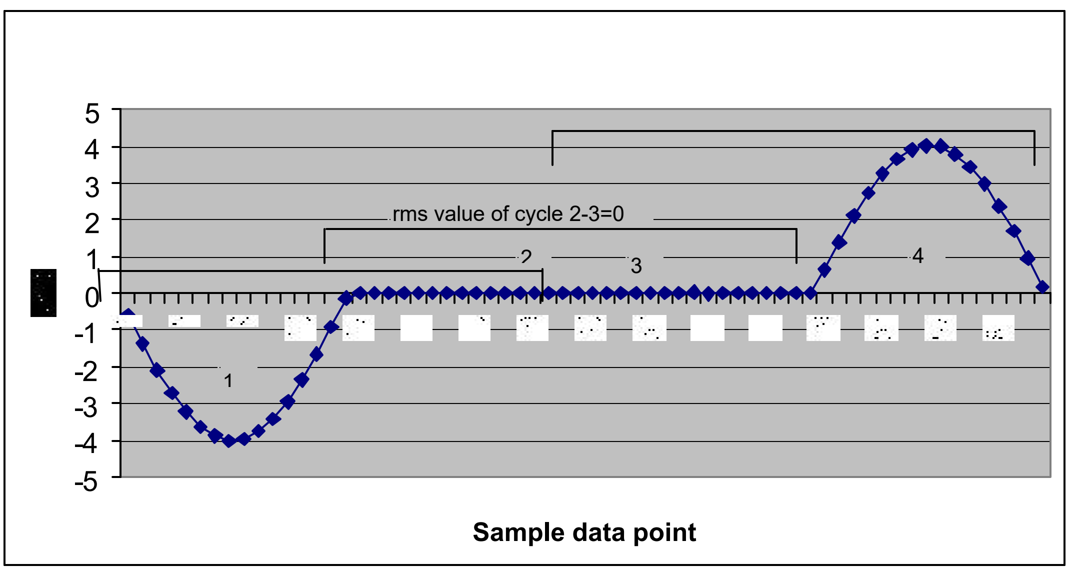
A 2 cycle, 90% voltage sag is shown in Figure 7.4. The voltage threshold is set to 95%. In the ideal case, the rms values recorded in the cycles 1-2 and 5-6 would be exactly 95% of the reference. The instrument will not record the sag in the cycles 1-2 and 5-6 shown in the figure. The sag will be recorded only in the half cycles 3,4 and 5. Therefore, the sag will be recorded for one and a half cycles instead of two cycles. In practice, due to the imperfections in the test waveforms, the actual rms value during the cycles 1-2 and 5-6 may be slightly over or under 95%. Accordingly the sag duration recorded can vary from one and a half cycles to three cycles. This is true in general for a sag of any duration with 90% retained voltage. Although the duration accuracy in this case does not meet Class A performance, this is not a serious limitation. Note that the threshold voltage for the testing purpose was set to 95%. This threshold is too high for a practical system. Threshold voltage in a practical power system is between 80% to 90%

of the reference voltage [4]. Any variation in the system voltage within 95% to 90% may not be considered as a sag at all. This variation would be considered as flicker instead of a sag. For sags with any other retained voltage, the instrument will record the sag duration within Class A accuracy limit. The last issue to be resolved is the retained voltage recorded by the instrument in the case of one cycle sags.

Unpredictable retained voltage measurement for one cycle sags

The fact that the process of data acquisition can begin at any arbitrary point on the waveform also causes uncertainty in the retained voltages measured in the case of one cycle sags. This point is illustrated by considering one cycle, 0% retained voltage sag shown in Figure 7.5.

Figure 7.5 One cycle, 0% retained voltage sag



If the data acquisition begins at the zero crossing of the waveform, the retained voltage recorded will be 0% (rms value of the cycle 2-3). But since the data acquisition can begin at any point over the wave, there is no guarantee that instrument will calculate this value. In one of the sample runs, the data acquired for a one- cycle 0% retained voltage sag by the instrument is shown in Figures 7.6(a) and 7.6(b).

Figure 7.6(a) Data acquisition not beginning at zero crossing

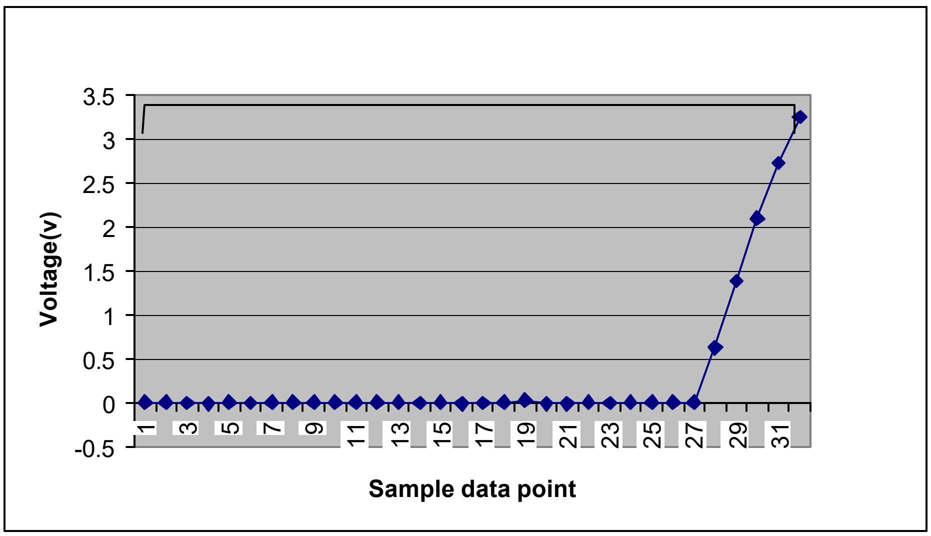
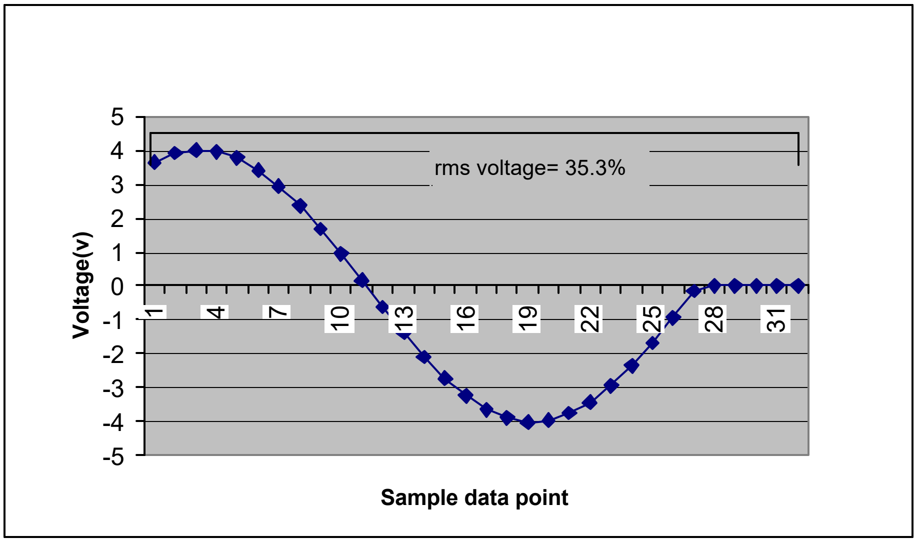


Figure 7.6(b) Data acquisition not beginning at zero crossing



The retained voltage calculated in this case is 35.3% and not zero. Therefore for any one cycle sag, the instrument will not be able to calculate the retained voltage accurately. For higher retained voltages, the error in the measurement will be less.

Again, it should be noted that one cycle sags do not occur often in practice. It usually takes longer than one cycle to clear any fault. For all the other sag durations, the instrument calculated retained voltages within Class A accuracy limit.

In conclusion, the performance of the sag monitoring instrument has been discussed in this chapter. The instrument performed satisfactorily on both the hardware setups. Sag duration and retained voltage measurement accuracy of the instrument satisfies Class A performance in most of the test cases. The errors recorded in some of the test cases are not a serious hindrance to the performance of the instrument.

CHAPTER VIII

CONCLUSION

The material presented in this document summarized the design and implementation of a sag monitoring and recording instrument based on a PC/104 embedded system architecture. Because the embedded architecture selected was a miniature version of a standard PC architecture, the learning curve was short. The hardware setup was designed to be light, small and environmentally rigid. The final hardware is about 420g in weight, about 3.6” • 3.8” • 3.5” in size and guaranteed to perform within a temperature range of 0°C to 55°C. If a DC/DC power supply is used, the temperature range is from -25°C to 50°C.

The instrument supports a complete operating system and high level programming language. This made application development faster and easier. Solid hardware and software support allowed fast and sophisticated double-buffered data acquisition for continuous monitoring. The application never failed due to any hardware or software error during testing.

The instrument implemented sag monitoring based on the IEC standards and there is no ambiguity regarding calculation or measurement of any of the parameters involved. The fact that most of the test results conform to Class A accuracy is an indicator of the stable design of the instrument. All the objectives that were established in Chapter I have been achieved.

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